

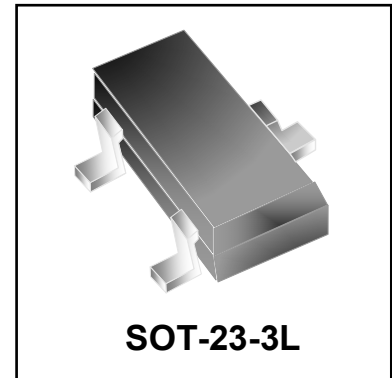
## P-Channel Enhancement MOSFET

### Features

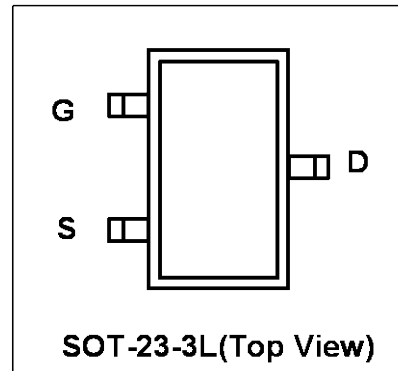
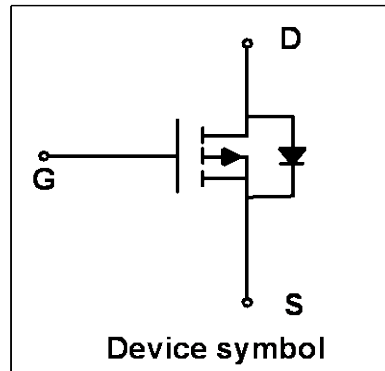
- Way-on Small Signal MOSFETs
- $V_{DS} = -30V$ ,  $I_D = -4.2A$   
 $R_{DS(on)} < 60m\Omega @ V_{GS} = -10V$   
 $R_{DS(on)} < 75m\Omega @ V_{GS} = -4.5V$
- Trench LV MOSFET Technology

### Mechanical Characteristics

- SOT-23-3L Package
- Marking : Making Code
- RoHS Compliant



### Schematic & PIN Configuration



### Absolute Maximum Rating ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D$	-4.2	A
$T_A=25^\circ C$			
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-16	A
Power Dissipation	$P_D$	1.5	W
$T_A=25^\circ C$			
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Ambient <sup>2</sup>	$R_{\theta JA}$	83.3	$^\circ C/W$

**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$	-	-	$\pm 100$	nA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.7	-1	-1.3	V
Drain-Source On-Resistance <sup>3</sup>	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -4.2A$	-	42	60	m $\Omega$
		$V_{GS} = -4.5V, I_D = -4A$	-	52	75	
		$V_{GS} = -2.5V, I_D = -1A$	-	60	90	
<b>Dynamic Characteristics<sup>4</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1MHz$	-	745	-	pF
Output Capacitance	$C_{oss}$		-	70	-	
Reverse Transfer Capacitance	$C_{rss}$		-	57	-	
<b>Switching Characteristics<sup>4</sup></b>						
Total Gate Charge	$Q_g$	$V_{GS} = -4.5V, V_{DS} = -15V,$ $I_D = -4.2A$	-	8	-	nC
Gate-Source Charge	$Q_{gs}$		-	1.8	-	
Gate-Drain Charge	$Q_{gd}$		-	2.7	-	
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DS} = -15V,$ $I_D = -4.2A, R_G = 6\Omega$	-	7	-	ns
Rise Time	$t_r$		-	3	-	
Turn-off Delay Time	$t_{d(off)}$		-	30	-	
Fall Time	$t_f$		-	12	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode forward voltage <sup>3</sup>	$V_{SD}$	$I_S = -4.2A, V_{GS} = 0V$	-	-	-1.2	V
Continuous Source Current	$I_S$		-	-	-4.2	A

**Notes:**

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^{\circ}\text{C}$
2. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse width $\leq 300\mu s$ , duty cycle $\leq 2\%$ .
4. This value is guaranteed by design hence it is not included in the production test.

### Typical Characteristics

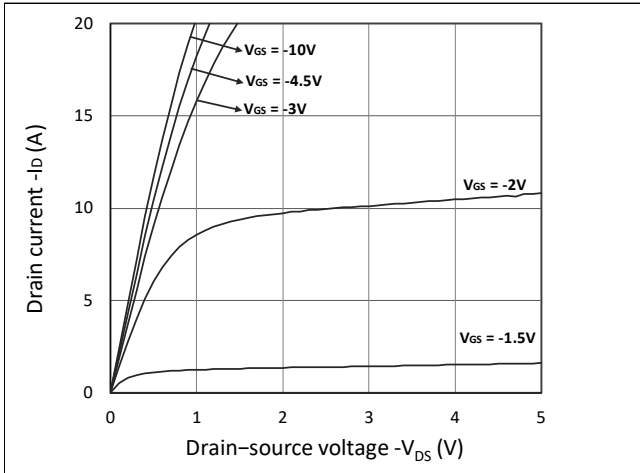


Figure 1. Output Characteristics

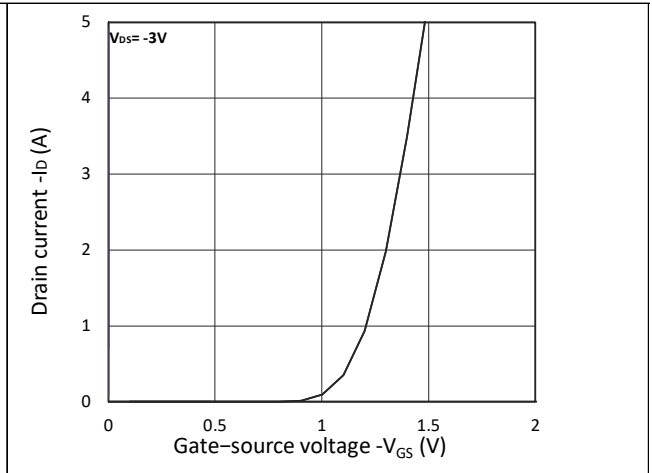


Figure 2. Transfer Characteristics

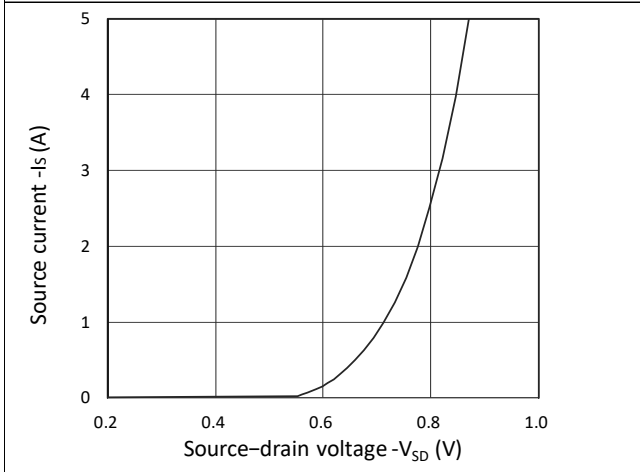


Figure 3. Forward Characteristics of Reverse

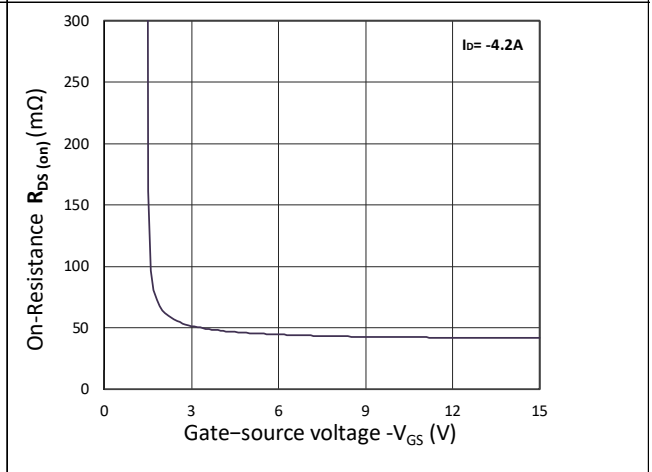


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

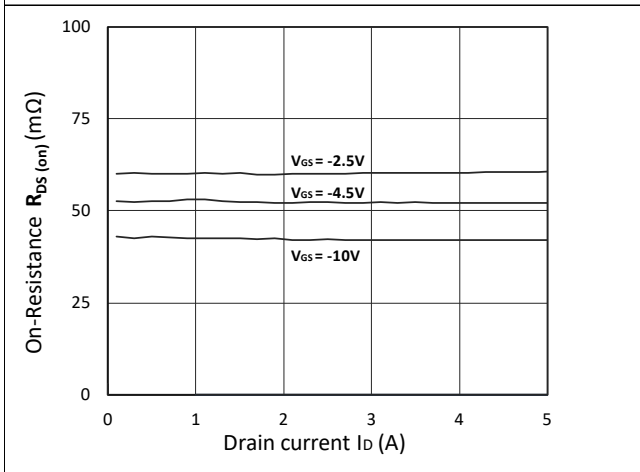


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

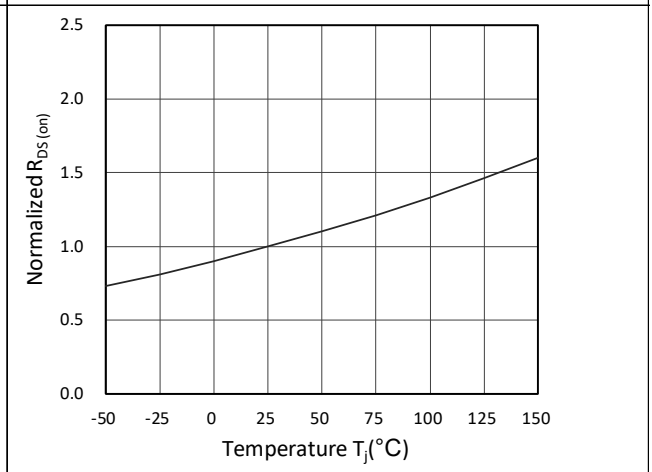


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

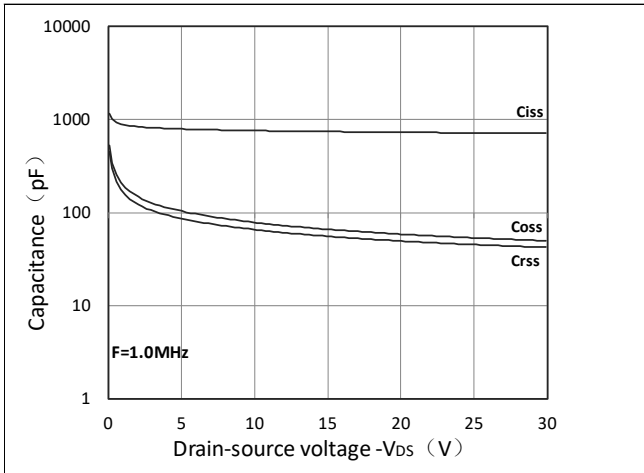


Figure 7. Capacitance Characteristics

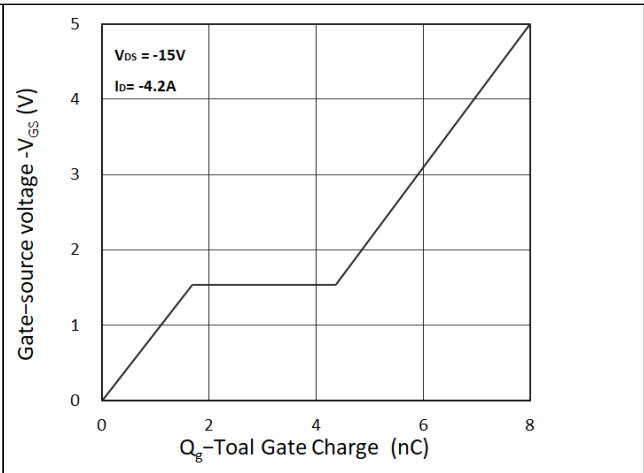
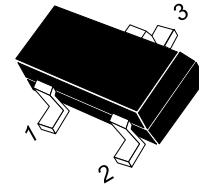
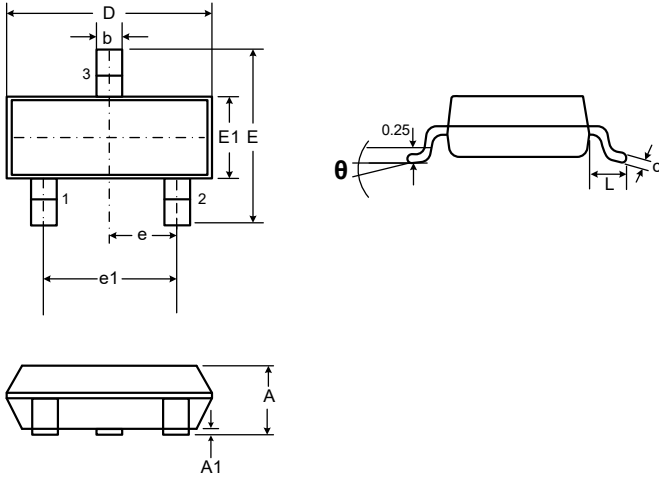


Figure 8. Gate Charge Characteristics

### Outline Drawing – SOT-23-3L

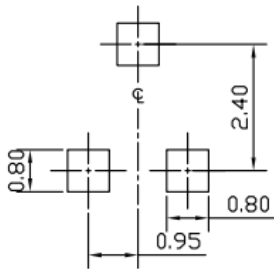
#### PACKAGE OUTLINE



SOT-23-3L

#### DIMENSIONS

SYMBOL	MILLIMETER		INCHES	
	MIN	MAX	MIN	MAX
A	1.05	1.30	0.041	0.051
A1	0.00	0.15	0.000	0.006
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.82	3.02	0.111	0.119
E	2.65	2.95	0.104	0.116
E1	1.50	1.70	0.059	0.067
e	0.95 BSC		0.0374 BSC	
e1	1.80	2.00	0.071	0.079
L	0.60REF		0.024REF	
θ	0	8°	0	8°



Unit:mm

#### Notes

1. Dimensioning and tolerances per ANSI Y14.5M, 1985.
2. Controlling Dimension: Inches
3. Dimensions are exclusive of mold flash and metal burrs.

### Marking Codes

Part Number	WM03P42M2
Marking Code	

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