3 to 5 Serial Cell Li-Ion / Li-Polymer Battery Protection IC with Temperature Protection

No.EA-514-220214

OVERVIEW

The R5651T is an overcharge and discharge protection IC for 3- to 5- series cell Li-ion / Li-polymer rechargeable battery pack, further includes a short-circuit and protection circuits for charge / discharge overcurrent. The R5651T can select any number of cells by applying a certain voltage on the SEL pin.

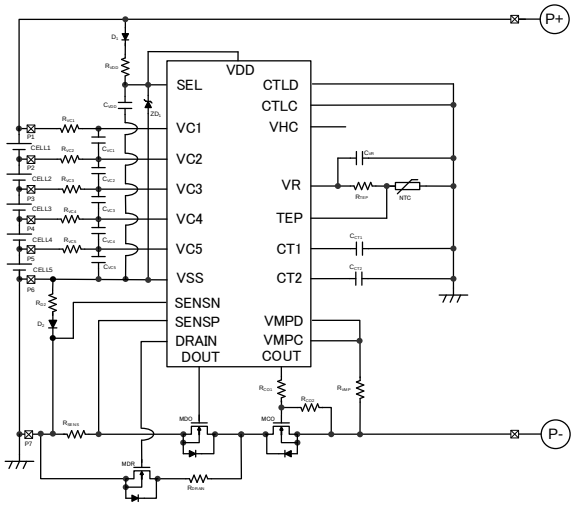
KEY BENEFITS

- Using a current-sense resistor with low resistance ratings: reduction in high temperature in large current and realizing a thermal design of a board easily
- Separation between charging and discharging paths: achieving low impedance of the battery pack
- Cascading: achieving simple circuit configuration for battery pack with six-cell and more and reducing external components

KEY SPECIFICATIONS

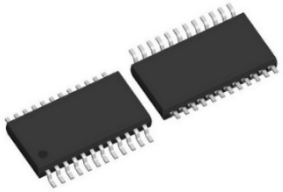
- High Voltage Tolerant Process
  Absolute maximum rating: 30V
- Low-consumption current
  Normal operation (5-cell): Typ.13.0 µA / Standby: Typ.6.0 µA
- High-accuracy Voltage Detection
  [Set voltage range, Accuracy, Delay time(t)]
  Overcharge detection voltage (V_{DET1n} (1)):
  3.60 V to 4.50 V, ±25 mV, t_{VDET1} = 1.0 sec
  Overcharge release voltage: V_{DET1n} - 0.1 V to V_{DET1n} - 0.4 V
  Overdischarge detection voltage (V_{DET2n} (1)):
  2.0 V to 3.2 V, ±50 mV, t_{VDET2}:OPT (2)
  Overdischarge release voltage: V_{DET2n} + 0.0 V to V_{DET2n} + 0.7 V
  - provided, Max. value is 3.2 V
  Discharge overcurrent detection voltage1 (V_{DET31}):
  0.010 V to 0.030 V, ±3 mV /
  0.035 V to 0.150 V, ±10%, t_{VDET31}: OPT (2)
  Discharge overcurrent detection voltage2 (V_{DET32}):
  0.030 V to 0.080 V, ±8 mV /
  0.090 V to 0.450 V, ±10%, t_{VDET32}: t_{VDET31}×1/10 or 1/20
  Charge overcurrent detection voltage (V_{DET4}):
  –0.008 V to -0.030 V, ±3 mV /
  –0.035 V to -0.050 V, ±10%, t_{VDET4} = 512 / 1024 / 2560 ms
  Short-circuit detection voltage(3):
  0.1 V to 0.6 V, ± 30%, t_{SHORT}: Typ. 330 µs
- 0 V Battery Charging Inhibition Voltage: 1.1 / 1.3 V, ±0.2 V
- Temperature Protection by NTC Thermistor
  Charge High setting: 45 / 50 / 55 / 60 °C, ±3°C
  Charge Low setting: –5 / –3 / 0 °C, ±3°C
  Discharge High setting: 65 / 70 / 75 °C, ±3°C
- Over-charge/discharge Release Type: Auto release
- Open-wire Detection Enabled
- Delay Time Shortening

TYPICAL APPLICATION CIRCUIT



5-cell Protection Circuit (CMOS output type)

PACKAGE



TSSOP-24

7.8 x 6.4 x 0.9 [mm]

APPLICATIONS

- Scooter (balance car) ● Cleaner
- Heat insulation box ● E-Bike ● Power tool

(1) V_{DET1n}, V_{DET2n}: n = 1, 2, 3, 4, 5
(2) Set by external capacitor
(3) V_{DET32} is not detected when V_{DET32} is higher than V_{SHORT}.

SELECTION GUIDE

Set voltages, Delay times and Optional functions are user selectable.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5651Txxx$∗-E2-FE	TSSOP-24	3,000 pcs	Yes	Yes

xxx: Specify the combination of the following set voltages. Refer to *Product Code List* for details.

V_{DET1n}[(1)]: 3.6 V to 4.5 V in 5 mV step
V_{REL1n}[(1)]: V_{DET1n} – 0.1 V to V_{DET1n} – 0.4 V in 50 mV step
V_{DET2n}[(1)]: 2.0 V to 3.2 V in 5 mV step
V_{REL2n}[(1)]: V_{DET2n} + 0.0 V to V_{DET2n} + 0.7 V in 100 mV step (Max. 3.2 V)
V_{DET31}: 0.010 V to 0.150 V in 5 mV step
V_{DET32}: 0.030 V to 0.450 V in 5 mV step
V_{SHORT}: 0.1 V to 0.6 V in 100 mV step
V_{DET4}: –0.008 V to –0.050 V in 5 mV step

$: Specify the charge overcurrent delay time (t_{VDET4}).

Delay Time Code Table

Code	t_{VDET32} [ms]	t_{VDET4} [ms]
A	t_{VDET31} × 1/10	512
C	t_{VDET31} × 1/10	1024

∗: Specify the combination of the following functions. Refer to *Function Code Table* for details.

Function Code Table

Code	Overdischarge Detection	0V Battery Charging	Open-wire Detection	Low-temp. Protection for charging
A	Auto Release	Inhibition	Enabled	Enabled

(1) V_{DET1n}, V_{REL1n}、V_{DET2n}, V_{REL2n} : n =1, 2, 3, 4, 5

Product Code List

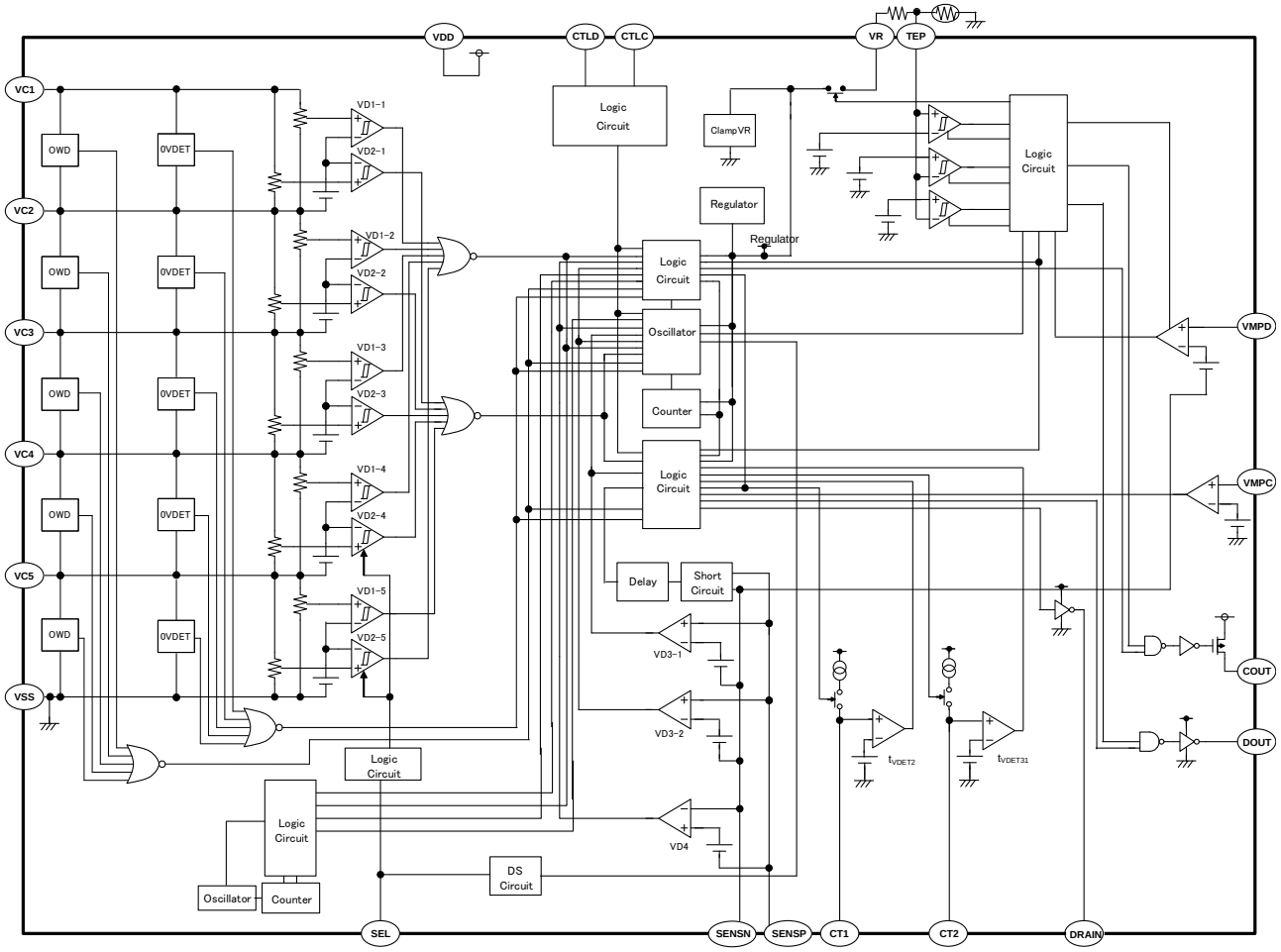
The product code is determined by a combination of the three digits set voltage code, the delay time code, and the function code.
The set voltage code is as following table. For more information on the delay and the selectable function codes, see *the Selection Guide chapter*.

Product Code Table

Product Name (Set Voltage Code [1])	Set Voltage [V]							Threshold Temperature (Release Temperature) [°C]		
	V_{DET1}	V_{DET2}	V_{DET31}	V_{DET32}	V_{DET4}	V_{SHORT}	V_{NOCHG}	T_{DCH}	T_{DCL}	T_{DDH}
R5651T**103**CA	4.250	2.750	0.100	0.200	–0.030	0.350	1.1	50 (45)	0 (5)	75 (70)
R5651T**104**CA	3.700	2.200	0.050	0.100	–0.030	0.300	1.3	55 (50)	0 (5)	75 (70)

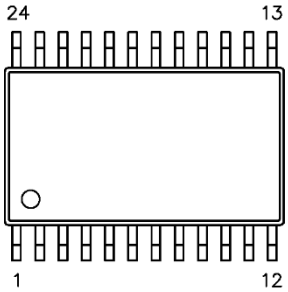
[1] Indicated with the numbers in bold type.

BLOCK DIAGRAM



R5651T Block Diagram

PIN DESCRIPTIONS



R5651T (TSSOP-24) Pin Configuration

R5651T Pin Description

Pin No	Symbol	Pin Description
1	VHC	Data transmission pin for VMPC input signal
2	CTLD	DOUT control pin
3	CTLC	COUT control pin
4	VC1	Positive terminal pin for CELL1
5	VC2	Positive terminal pin for CELL2
6	VC3	Positive terminal pin for CELL3
7	VC4	Positive terminal pin for CELL4
8	VC5	Positive terminal pin for CELL5
9	VSS	Ground pin for the IC
10	SENSN	Current sense pin, negative
11	SENSP	Current sense pin, positive
12	DRAIN	FET's gate connection pin for discharge overcurrent release voltage
13	DOUT	Overdischarge detection output pin, CMOS output
14	COUT	Overcharge detection output pin, PMOS open-drain output
15	VMPD	Current load negative input pin
16	VMPC	Charger negative input pin
17	N.C.	No Connection
18	VR	Internal VR output pin
19	TEP	Thermistor reference input voltage pin
20	CT1	Capacitor (C_{CT1}) connection pin for t_{VDET2n}
21	CT2	Capacitor (C_{CT2}) connection pin for t_{VDET31}
22	N.C.	No Connection
23	SEL	3- / 4- / 5-cell selectable pin
24	VDD	Power supply pin

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, VSS = 0 V)

Symbol	Parameter	Rating	Unit
V_{DD}	Power Supply Voltage	–0.3 to 30	V
V_{VC1}	VC1 Pin Input Voltage	0.3 to 30	V
V_{VCn}	VCn (n = 2,3,4) Pin Input Voltage	V_{VCn+1} – 0.3 to V_{VCn-1} + 0.3	V
V_{VC5}	VC5 Pin Input Voltage	–0.3 to V_{VC4} + 0.3	V
V_{VMPC}	VMPC Pin Input Voltage	V_{DD} – 30 to V_{DD} + 0.3	V
V_{VMPD}	VMPD Pin Input Voltage	V_{DD} – 30 to V_{DD} + 0.3	V
V_{SEL}	SEL Pin Input Voltage	V_{DD} – 30 to V_{DD} + 0.3	V
V_{SENSN}	SENSN Pin Input Voltage	V_{DD} – 30 to V_{VR} + 0.3	V
V_{SENSP}	SENSP Pin Input Voltage	V_{DD} – 30 to V_{VR} + 0.3	V
V_{CT1}	CT1 Pin Input Voltage	–0.3 to 6.5	V
V_{CT2}	CT2 Pin Input Voltage	–0.3 to 6.5	V
V_{TEP}	TEP Pin Input Voltage	–0.3 to 6.5	V
V_{CTLC}	CTLC Pin Input Voltage	–0.3 to V_{DD} + 25 < 48	V
V_{CTLD}	CTLD Pin Input Voltage	–0.3 to V_{DD} + 25 < 48	V
V_{COUT}	COUT Pin Output Voltage	V_{DD} – 30 to V_{DD} + 0.3	V
V_{DOUT}	DOUT Pin Output Voltage	–0.3 to V_{OH2} + 0.3	V
V_{DRAIN}	DRAIN Pin Output Voltage	–0.3 to V_{OH3} + 0.3	V
V_{VR}	VR Pin Output Voltage	–0.3 to V_{VR} + 0.3	V
V_{VHC}	VHC Pin Output Voltage	V_{DD} – 3 to V_{DD} + 4 < 30	V
P_D	Power Dissipation	Refer to Appendix “Power Dissipation”	
Tj	Junction Temperature Range	–40 to 125	°C
Tstg	Storage Temperature Range	–55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Rating	Unit
V_{DD}	Operating Input Voltage	4.0 to 25.0	V
Ta	Operating Temperature Range	–40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{CELLn} n = 1, 2, 3, 4, 5 (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), unless otherwise noted.

R5651Txxxxx Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Conditions		Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Circuit (1)
V_{DET1n}	CELLn overcharge detection voltage	at rising edge of VDD		V_{DET1n} – 0.025	V_{DET1n}	V_{DET1n} + 0.025	V	A
V_{REL1n}	CELLn overcharge release voltage	at falling edge of VDD		V_{REL1n} – 0.050	V_{REL1n}	V_{REL1n} + 0.050	V	A
t_{VDET1}	Overcharge detection delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 3.4 V → V_{DET1n}+0.2 V		0.7	1.0	1.3	s	B
t_{VREL1}	Overcharge release delay time	V_{DD} = V_{VC1} V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = V_{DET1n}+0.2 V→ 3.4 V		11	16	21	ms	B
V_{DET2n}	CELLn overdischarge detection voltage	at falling edge of VDD		V_{DET2n} – 0.050	V_{DET2n}	V_{DET2n} + 0.050	V	C
V_{REL2n}	CELLn overdischarge release voltage	at rising edge of VDD		V_{REL2n} – 0.050	V_{REL2n}	V_{REL2n} + 0.050	V	C
t_{VDET2}	Overdischarge detection delay time	t_{VDET2A} = C_{CT1} × V_{DCT1} / I_{CT1}, C_{CT1A} = 33 nF		85	120	163	ms	-
I_{CT1}	CT1 pin charge current	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 3.4 V → 1.5 V		350	500	650	nA	D
V_{DCT1}	CT1 pin detection voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 1.5 V		1.44	1.80	2.16	V	E
t_{VREL2}	Overdischarge release delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5), V_{CELL1} = 1.5 V → 3.4 V		0.7	1.5	2.6	ms	C
V_{DET31}	Discharge overcurrent detection voltage1	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{VMPD} = 4.0 V, V_{SENSN} = 0 V, at rising edge of SENSP	V_{DET31} < 0.03	V_{DET31} –0.003	V_{DET31}	V_{DET31} +0.003	V	F
			V_{DET31} ≥ 0.035	V_{DET31} –10%		V_{DET31} +10%		
V_{DET32}	Discharge overcurrent detection voltage2	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{VMPD} = 4.0 V, V_{SENSN} = 0 V, at rising edge of SENSP	V_{DET32} < 0.08	V_{DET32} –0.008	V_{DET32}	V_{DET32} +0.008	V	F
			V_{DET32} ≥ 0.09	V_{DET32} –10%		V_{DET32} +10%		
V_{SHORT}	Short protection voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{VMPD} = 4.0 V, V_{SENSN} = 0 V, at rising edge of SENSP		V_{SHORT} –30.0%	V_{SHORT}	V_{SHORT} +30.0%	V	F
V_{REL3}	Discharge overcurrent release voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{SENSN} = 0 V, V_{SENSP} = 0 V, at falling edge of VMPD		0.8	1.0	1.2	V	F

(1) Refer to *TEST CIRCUITS* for detail information.

R5651T Electrical Characteristics (continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Circuit (1)
I_{CT2}	CT2 pin charge current	$V_{DD} = V_{VC1}, V_{CELLn}$ = 3.4 V, V_{SENSN} = 0V, V_{SENSP} = 0V → V_{DET31} + 0.005 V	350	500	650	nA	G
V_{DCT2}	CT2 pin charge detection voltage	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{SENSN} = 0 V, V_{SENSP} = V_{DET31} + 0.005 V, V_{VMPD} = 4.0 V	1.20	1.50	1.80	V	H
t_{VDET31}	Discharge overcurrent delay time1	$t_{VDET31} = C_{CT2} \times V_{DCT2}/I_{CT2}$ C_{CT2} = 3.3 nF	6.9	9.9	12.9	ms	-
t_{VDET32}	Discharge overcurrent delay time2	t_{VDET31} × 1/10: $t_{VDET32} = C_{CT2} \times V_{DCT2}/ (I_{CT2} \times 10)$ C_{CT2} = 3.3 nF	0.69	0.99	1.29	ms	-
		t_{VDET31} × 1/20: $t_{VDET32} = C_{CT2} \times V_{DCT2}/ (I_{CT2} \times 20)$ C_{CT2} = 3.3 nF	0.34	0.495	0.65		
t_{SHORT}	Short-circuit detection delay time	$V_{DD} = V_{VC1}, V_{CELLn}$ = 3.4 V, V_{SENSN} = 0 V, V_{SENSP} = 0 V → 1.5 V, V_{VMPD} = 3.0 V	230	330	450	µs	F
t_{VREL3}	Discharge overcurrent release delay time	$V_{DD} = V_{VC1}, V_{CELLn}$ = 3.4 V V_{SENSN} = 0 V, V_{SENSP} = 0 V, V_{VMPD} = 4.0 V → 0V	2.8	4	5.85	ms	F
V_{DET4}	Charge overcurrent detection voltage4	$V_{DD} = V_{VC1}, V_{CELLn}$ = 3.4 V, V_{VMPD} = −1.0 V, V_{SENSP} = 0 V, at falling edge of SENSP; $V_{DET4} \geq -0.03$	V_{DET4} –0.003	V_{DET4}	V_{DET4} + 0.003	V	I
		$V_{DET4} < -0.03$	V_{DET4} –10%		V_{DET4} + 10%		
V_{REL4}	Charge overcurrent release voltage	$V_{DD} = V_{VC1}, V_{CELLn}$ = 3.4 V, at rising edge of VMPC	0.05	0.1	0.15	V	I
t_{VDET4}	Charge overcurrent delay time	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V, V_{SENSN} = 0 V, V_{SENSP} = 0V → −1.0 V	t_{VDET4} –37.5%	t_{VDET4}	t_{VDET4} +37.5%	ms	I
t_{VREL4}	Charge overcurrent release delay time	$V_{DD} = V_{VC1}, V_{CELLn}$ = 3.4 V, SENS = 0 V, V_{SENSP} = 0V, V_{VMPC} = −1.0 V →1.0 V	2.8	4	5.85	ms	I
V_{IH}	SEL pin input voltage, high	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V	V_{VDD} – 0.3		V_{VDD} + 0.3	V	J
V_{IM}	SEL pin input voltage, middle	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V	2.0		V_{DD} - 2.0	V	J
V_{IL}	SEL pin input voltage, low	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V	V_{VSS} – 0.3		V_{VSS} + 0.3	V	J

(1) Refer to *TEST CIRCUITS* for detail information.

R5651T Electrical Characteristics (continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
			Min.	Typ.	Max.		
V_{OL2}	DOUT pin NMOS ON voltage	I_{OL} = 50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V		0.02	0.1	V	K
V_{OL3}	DRAIN pin NMOS ON voltage	I_{OL} = 50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V		0.04	0.2	V	L
V_{OH1}	COUT pin PMOS ON voltage	I_{OH} = −50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} – 0.5	V_{DD} – 0.1		V	M
V_{VR}	VR pin output voltage	V_{VDD} = V_{VC1}, V_{CELLn} = 3.4 V	3.5	3.6	3.7	V	N
V_{VR12}	VR pin 12V output voltage	I_{OH} = −5 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, Measured to draw the current through DOUT	9.5	12	14	V	O
V_{OH2}	DOUT pin PMOS ON voltage (2)	I_{OH} = −50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{VR12} – 0.5	V_{VR12} – 0.1		V	O
V_{OH3}	DRAIN pin PMOS ON voltage (2)	I_{OH} = −50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{SENSN} = 0 V V_{SENSP} = V_{VMPD} = 4.0 V	V_{VR12} – 0.5	V_{VR12} – 0.1		V	P
I_{LCOUT}	COUT pin off leak current	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, C_{OUT} = −13 V	– 0.1			µA	Q
T_{DCH}	Charge high-temperature detection temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DCH} – 3	T_{DCH}	T_{DCH} + 3	°C	R
T_{RCH}	Charge high-temperature release temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DCH} – 10	T_{DCH} – 5	T_{DCH}	°C	R
t_{TDCH}	Charge high-temperature detection delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4V, V_{TEP} = 0.9 V → 0.3 V	44	64	84	ms	R
t_{TRCH}	Charge high-temperature release delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4V, V_{TEP} = 0.3 V → 0.9 V	44	64	84	ms	R
T_{DCL}	Charge low-temperature detection temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DCL} – 3	T_{DCL}	T_{DCL} + 3	°C	R
T_{RCL}	Charge low-temperature release temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DCL} – 10	T_{DCL} – 5	T_{DCL}	°C	R
t_{TDCL}	Charge low-temperature detection delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{TEP} = 0.9 V → 3.5 V	44	64	84	ms	R
t_{TRCL}	Charge low-temperature release delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{TEP} = 3.5 V → 0.9 V	44	64	84	ms	R

(1) Refer to *TEST CIRCUITS* for detail information.

(2) If the VDD pin voltage becomes lower than the output of the regulator, the output voltage (DOUT, DRAIN) becomes almost equal to V_{DD}.

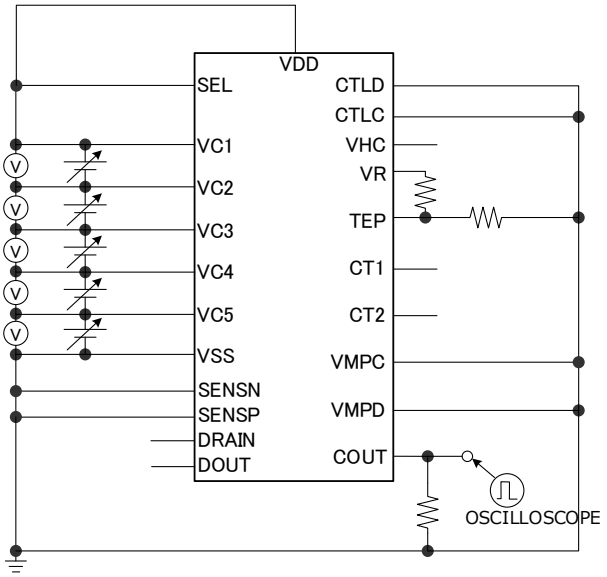
R5651T Electrical Characteristics (continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
			Min.	Typ.	Max.		
T_{DDH}	Discharge high-temperature detection temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DDH} – 3	T_{DDH}	T_{DDH} + 3	°C	R
T_{RDH}	Discharge high-temperature release temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DDH} – 10	T_{DDH} – 5	T_{DDH}	°C	R
t_{TDDH}	Discharge high-temperature detection delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4V, V_{VTEP} = 0.9 V → 0 V	44	64	84	ms	R
t_{TRDH}	Discharge high-temperature release delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{VTEP} = 0 V → 0.9 V	44	64	84	ms	R
t_{VTT}	Temperature scanning cycle	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	0.7	1	1.3	s	S
V_{DSG}	Discharge detection voltage	(V_{VMPD} – V_{SENSN}) increasing	5	10	15	mV	T
V_{NOCHGn}	0 V battery charging inhibition voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.2 V	V_{NOCHGn} – 0.2	V_{NOCHGn}	V_{NOCHGn} + 0.2	V	A
t_{LT}	Open-wire scanning cycle time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	2.8	4	5.2	s	U
V_{CTLC1H}	CTLC pin high threshold voltage 1	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} + 0.3	V_{DD} + 1.1	V_{DD} + 2.0	V	V
V_{CTLC2H}	CTLC pin high threshold voltage 2	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} – 2.2	V_{DD} – 1.1	V_{DD} – 0.1	V	V
V_{CTLD1H}	CTLD pin high threshold voltage 1	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} + 0.3	V_{DD} + 1.1	V_{DD} + 2.0	V	W
V_{CTLD2H}	CTLD pin high threshold voltage 2	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} – 3.95	V_{DD} – 2.75	V_{DD} – 1.6	V	W
t_{CTLD1}	CTLD pin input delay time 1	V_{DD} = V_{VC1}, V_{CELLn} = 3.4V, V_{CTLD} = V_{DD}+0.5 V→V_{DD}+1.7 V	0.7	1.5	2.6	ms	W
t_{CTLD2}	CTLD pin input delay time 2	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{CTLD} = V_{DD}+1.7 V → V_{DD}+0.5 V	2.45	3.50	4.55	ms	W
t_{CTLC1}	CTLC pin input delay time 1	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{CTLC} = V_{DD} → V_{DD} +2.0V	0.7	1.5	2.6	ms	V
t_{CTLC2}	CTLC pin input delay time 2	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{CTLC} = V_{DD}+2.0 V → V_{DD}	3.15	4.5	5.85	ms	V
I_{SS1}	Supply current 1	V_{DD} = VC1, COUT = OPEN V_{CELLn} = V_{DET1n} – 0.4 V		13	30	µA	X
I_{SS2}	Supply current 2	V_{DD} = VC1, COUT = OPEN V_{CELLn} = 1.5 V		6	12	µA	X
V_{STB}	Standby mode turned-on voltage	V_{DD} = VC1 = 1.5 V, V_{CELLn} = 3.4 V, At rising edge of VMPD	0.05	0.1	0.15	V	X

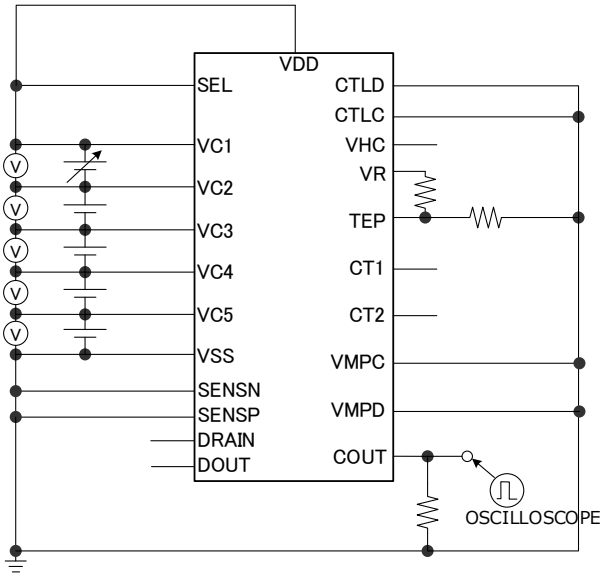
(1) Refer to *TEST CIRCUITS* for detail information.

Test Circuits

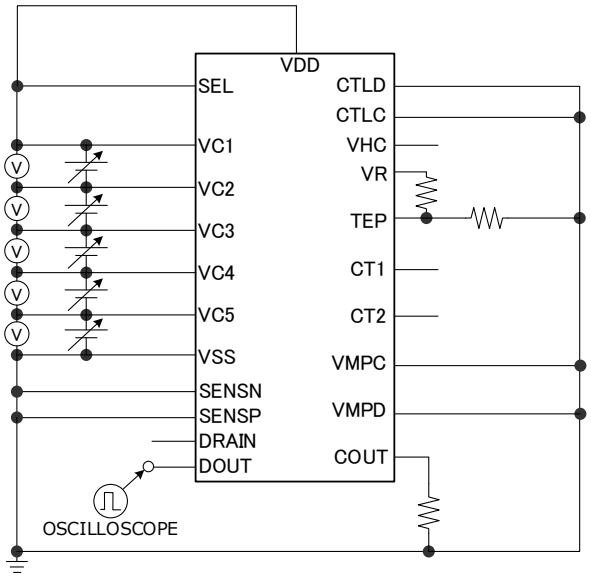
A



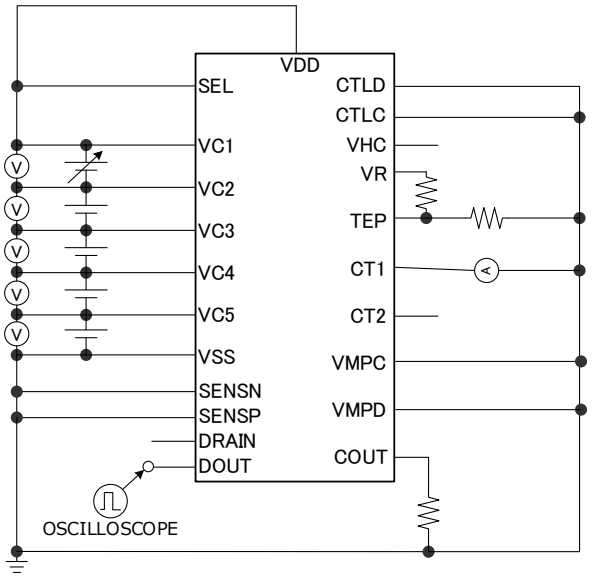
B



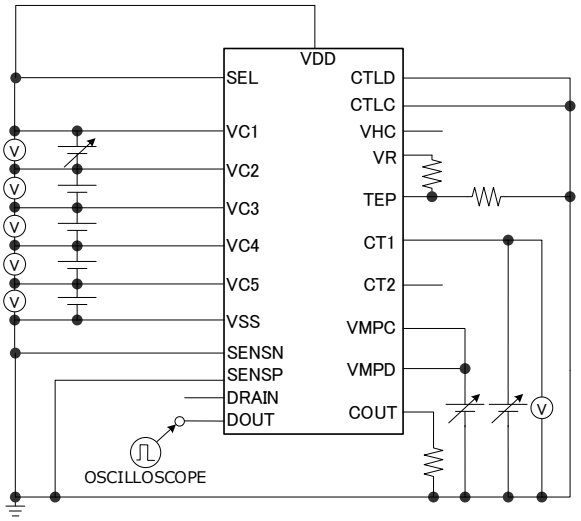
C



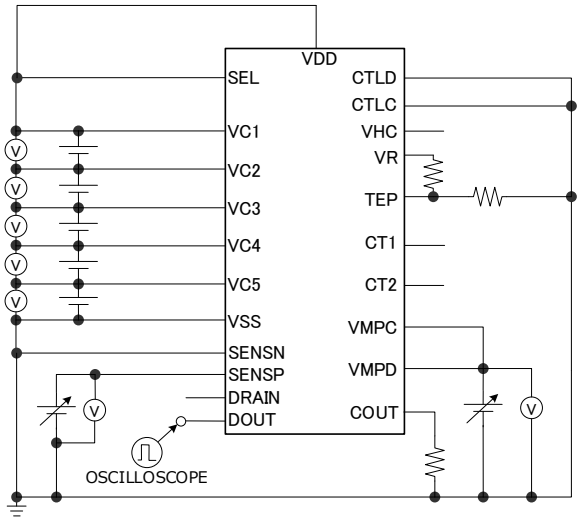
D



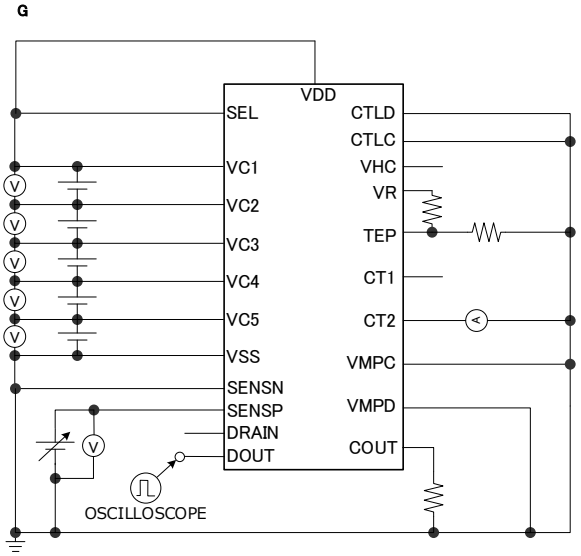
E


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

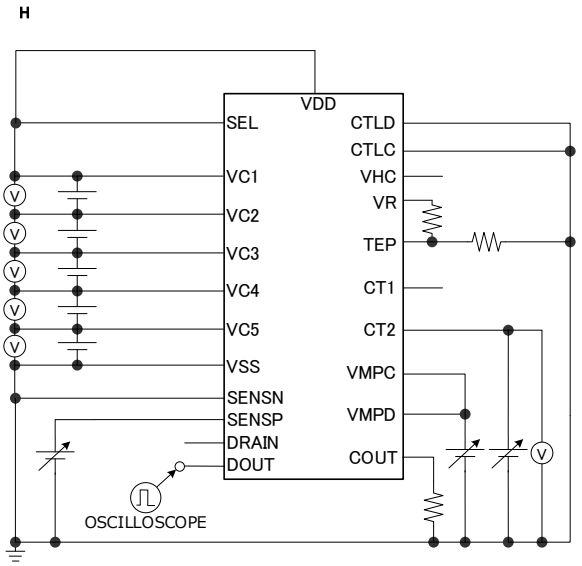
F


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

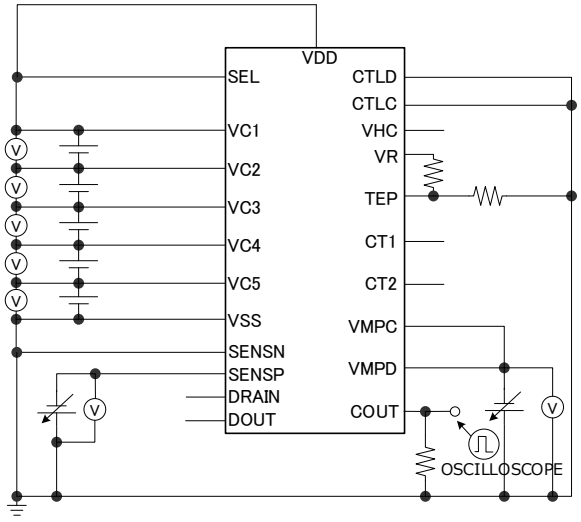
G


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

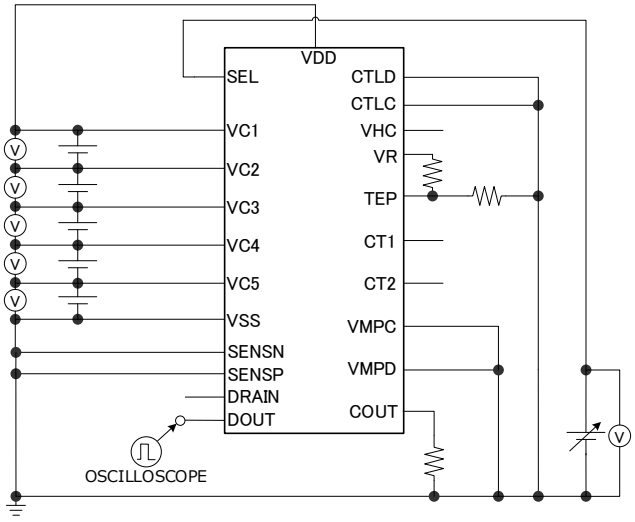
H


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

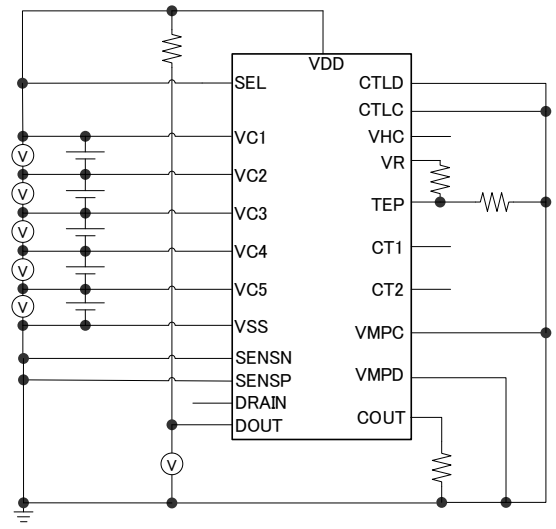
I


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

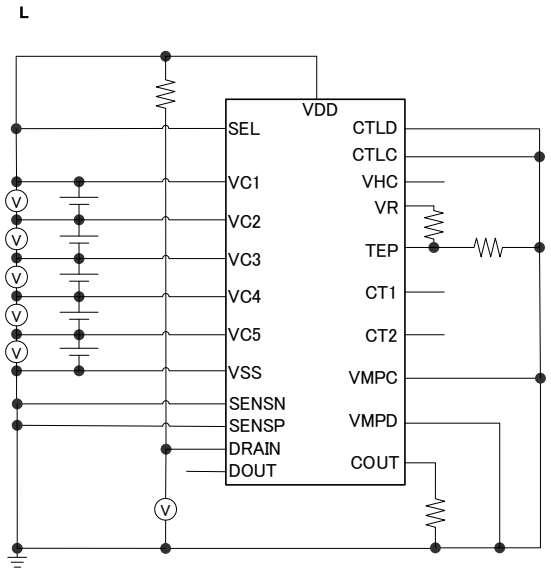
J


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

K


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT

L


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
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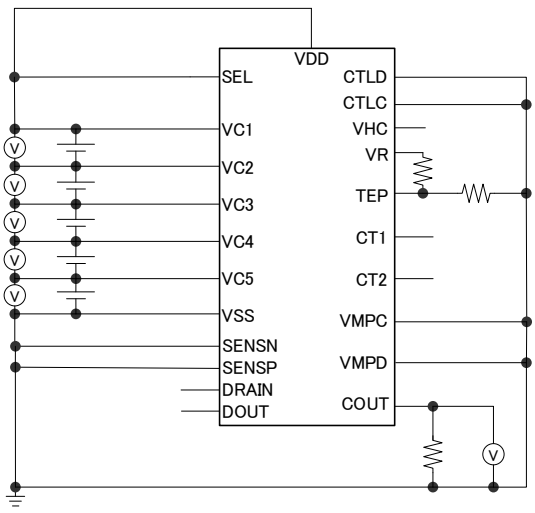
VMPC
VMPD
COUT

M


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
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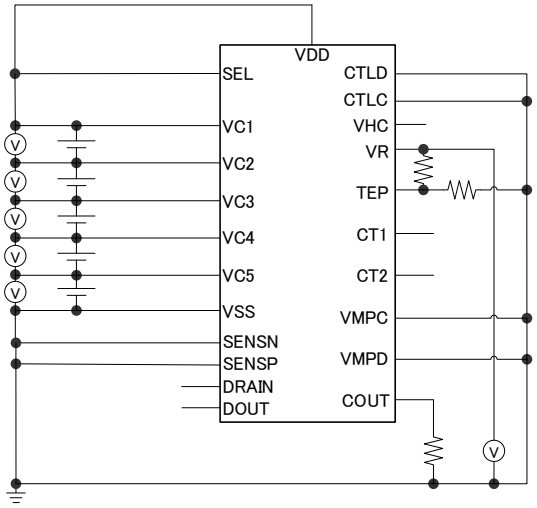
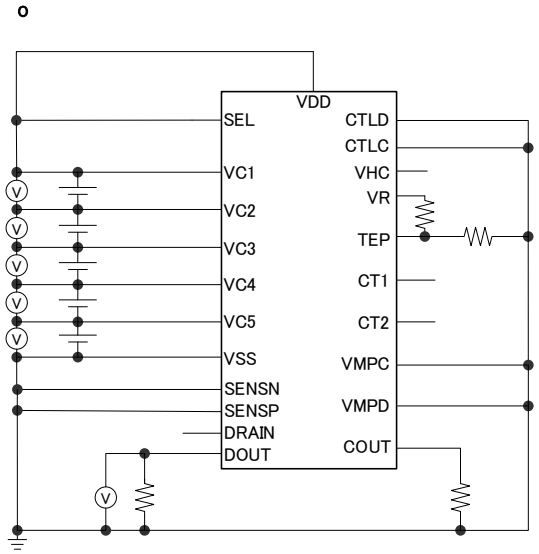
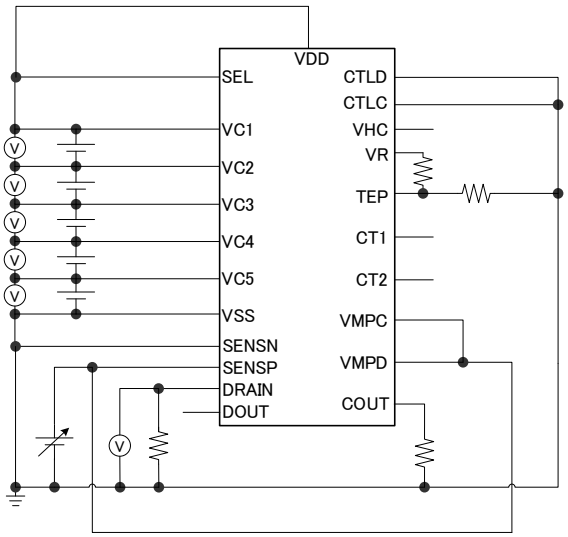
N


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
V

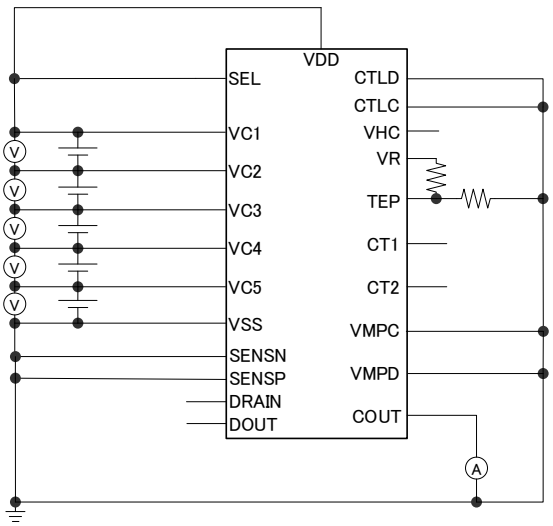
O


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
V

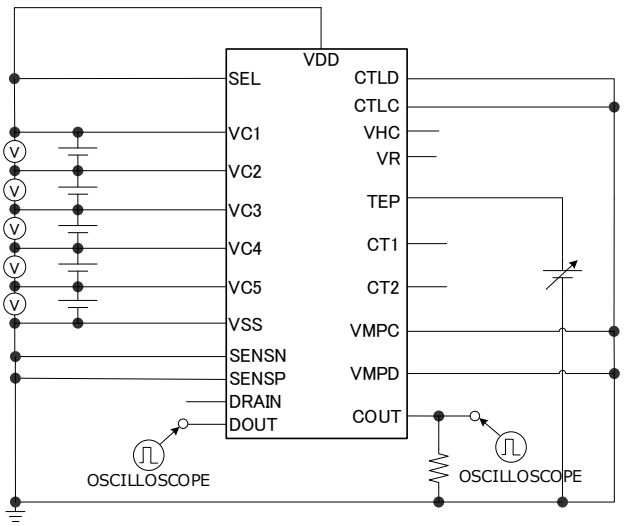
P


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
V

Q


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
A

R


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE
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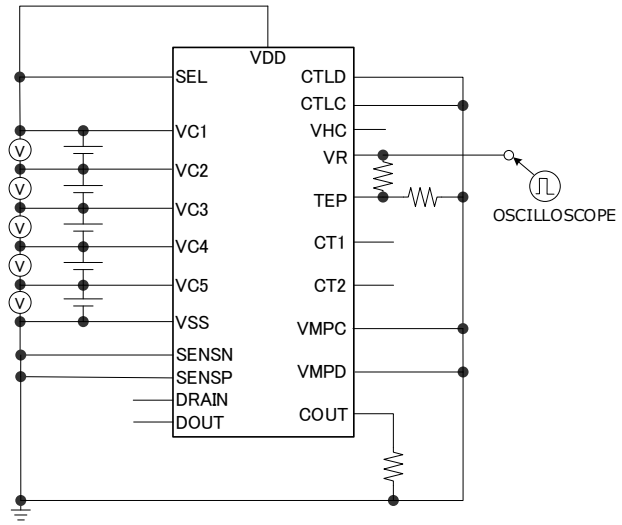
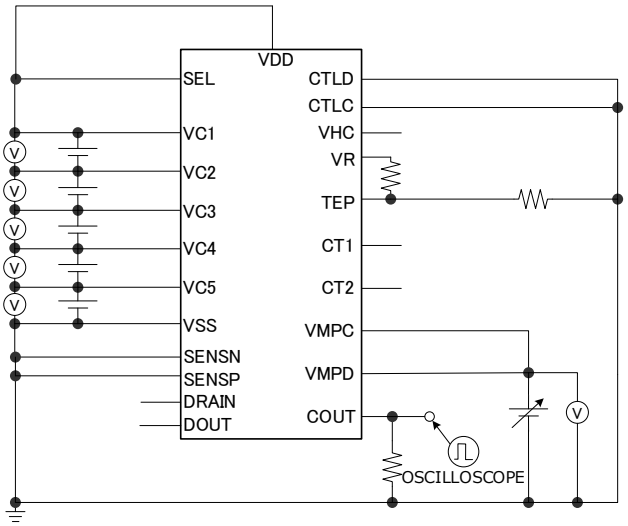
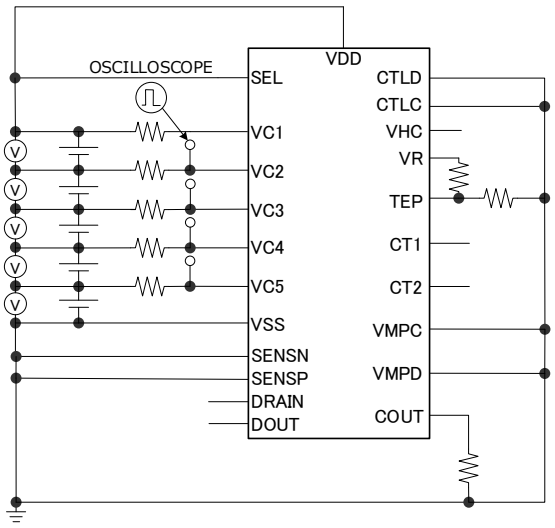
S


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

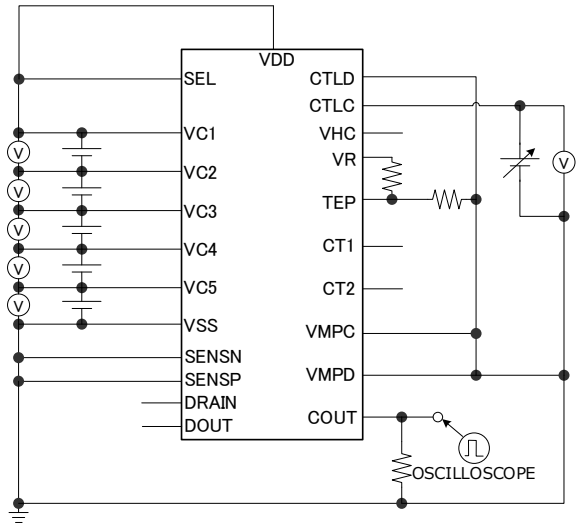
T


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

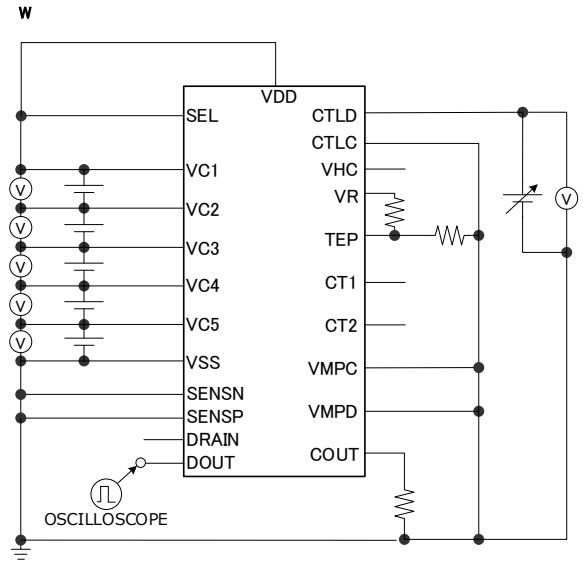
U


OSCILLOSCOPE
VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT

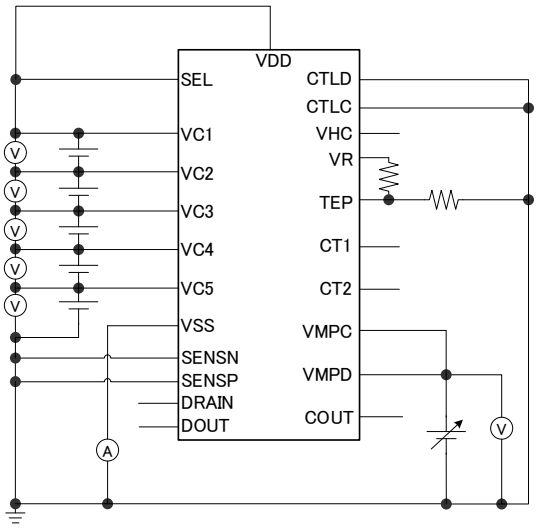
V


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

W


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
VR
TEP
CT1
CT2
VMPC
VMPD
COUT
OSCILLOSCOPE

X


VDD
SEL
VC1
VC2
VC3
VC4
VC5
VSS
SENSN
SENSP
DRAIN
DOUT
CTLD
CTLC
VHC
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THEORY OF OPERATION

Overcharge Detection: VD1n (n = 1, 2, 3, 4, 5)

When charging, the R5651T supervises voltages between VC1 and VC2, VC2 and VC3, VC3 and VC4, VC4 and VC5, and VC5 and VSS pins, respectively, they are assigned to the CELL1 to 5 voltages.

When at least one of the cell voltages exceeds the overcharge detection voltage, the IC enters the overcharged state and the COUT pin connected to an external pull-down resistor becomes Hi-z. Thereby, the charging stops when the external Nch FET is turned off.

After the overcharge detection, when all the cell voltages drop below the overcharge detection voltage (V_{DET1n}) with load, or when all the cell voltages drop below the overcharge release voltage (V_{REL1n}) without load, the COUT pin becomes High and the charging is available.

The overcharge detection and release delay times (t_{VDET1}, t_{VREL1}) are fixed internally. The IC enters the overcharged state when t_{VDET1} passes while the at least one of the cell voltages exceeds V_{DET1n}. However, the IC does not enter when all the cell voltages drop below V_{DET1n} within t_{VDET1}.

Besides, the IC does not release from the overcharged state when at least one of the cell voltages exceeds V_{REL1n} within t_{VREL1} after the overcharge detection even when all the cell voltages drop below V_{REL1n}. The COUT pin of the Pch open-drain output type outputs the VDD pin voltage at High.

Overdischarge Detection: VD2n (n = 1, 2, 3, 4, 5)

When discharging as with the overcharge, the R5651T supervises voltages the CELL1 to 5 voltages in the overdischarged state. When at least one of the cell voltages drops below the overdischarge detection voltage (V_{DET2n}), the IC enters the overdischarged state and the DOUT pin becomes “Low”. Thereby, the discharging stops when the external Nch FET is turned off. When the cell voltage exceeds VREL2n, the IC releases from the overdischarged state without the charger and the DOUT pin voltage becomes High.

The overdischarge detection delay time (t_{VDET2}) is settable. t_{VDET2} is set by the external capacitor (C_{CT1}) connected to the CT1 pin. The IC enters the overdischarged state when t_{VDET2} passes while the at least one cell voltage drops below V_{DET2n}. However, the IC does not go to the overdischarged when all the cell voltages exceed V_{DET2n} within t_{VDET2}. The overdischarge release delay time (t_{VREL2}) is fixed internally.

Besides, the IC does not release from the overdischarged state when at least one of the cell voltages drops below V_{REL2n} within t_{VREL2} even when all the cell voltages exceed V_{REL2n} after the overdischarge detection.

In the case that the VMPD pin voltage (V_{VMPD}) becomes High after the overdischarge detection, the IC stops circuits not required to reduce the power consumption to a minimum. The DOUT pin of CMOS output type outputs approx.12V from the internal regulator at High and the VSS pin voltage at Low.

When the overdischarge detection overlaps the open-wire detection, the overdischarge detection starts firstly, after that, the open-wire detection starts.

Discharge Overcurrent Detection: VD3n (n = 1, 2) and Short-circuit Detection

In the discharge enabled state, the R5651T supervises the SENSP pin voltage (V_{SENSP}) with reference to the SENSN voltage and enters the discharge overcurrent detected state when V_{SENSP} becomes from the discharge overcurrent detection voltage (V_{DET3n}) under the short-circuit detection voltage (V_{SHORT}) due to a large load. The DOUT pin becomes Low and thereby it prevents to apply a large current when the external FET is turned off.

The discharge overcurrent is detected in two steps (V_{DET31} / V_{DET32}). The discharge overcurrent detection delay time 1/2 (t_{VDET31} / t_{VDET32}) for V_{DET31} / V_{DET32} are settable. t_{VDET31} is set by the external capacitor (C_{CT2}) connected to the CT2 pin and t_{VDET32} is set to become one-tenth or one-twenty of t_{VDET31}. The IC does not entry the discharge overcurrent detected state when V_{SENSP} drops below V_{DET3n} within the delay time. The discharge overcurrent release delay time (t_{VREL3}) and the short-circuit detection delay time (t_{SHORT}) is fixed internally.

An external resistor for the discharge overcurrent release must be set among each drain of the external FETs connected to the DRAIN, COUT, and DOUT pins. After the discharge overcurrent or short-circuit detection, it is required that the external FET connected to the DRAIN pin is turned on and the resistor for the overcurrent release is connected to V_{SS}. When the load is released after the detection, the VMPD pin voltage (V_{VMPD}) is pulled down to VSS via the resistor for the overcurrent release, and thereby V_{VMPD} drops below V_{REL3}.

After a certain delay time, the discharge overcurrent or short-circuit detected state is released. When the discharge overcurrent detection is released, the external FET connected to the DRAIN pin is turned off and the resistor for the overcurrent release is disconnected from V_{SS}.

Charge Overcurrent Detection: VD4

In the charge / discharge enabled state, the R5651T supervises the SENSP pin voltage (V_{SENSP}) with reference to the SENSN voltage. A large current is applied by connecting an inappropriate charger, and the IC enters the charge overcurrent detected state when the SENSP pin voltage (V_{SENSP}) becomes the charge overcurrent detection voltage (V_{DET4}) or less. Thereby, the COUT pin with an external pull-down resistor becomes Hi-Z and it prevents to apply the large current to the circuits when the external Nch FET is turned off.

The IC does not enter the charge overcurrent detected state when V_{SENSP} exceeds V_{DET4} within a delay time. The delay times for the charge overcurrent detection / release is fixed internally.

The VMPC pin voltage (V_{VMPC}) exceeds the charge overcurrent release voltage (V_{REL4}) when a load is connected after disconnecting the charger, and the IC is released from the charge overcurrent detected state after passing the charge overcurrent release delay time (t_{VREL4}).

0 V Battery Charging Inhibition: V_{NOCHGn} (n = 1, 2, 3, 4, 5)

The R5651T detects the charge inhibition voltage (V_{NOCHG}) for each cell. When any one of the cell voltages drops below V_{NOCHG}, the charge inhibition is detected with the charger connected to the battery pack. Thereby, the COUT pin become Hi-Z and stop to charge.

Standby Mode

In the overdischarge detected state, the R5651T shifts from normal mode to standby mode while the VMPD pin voltage (V_{VMPD}) exceeds the standby mode detection voltage (V_{STB}). In the standby mode, the IC stops circuits not required to reduce the power consumption to a minimum. This IC can return from the standby mode to the normal mode when V_{VMPD} drops below V_{STB} by connecting the charger.

Operating Mode Switching by SEL Pin

The SEL pin is a selectable switching pin for three- to five-cell protection modes.

Operating Modes

Reference input voltage level for SEL pin	Modes
VDD pin voltage level	5-cell protection
VC4 pin voltage level: (V_{DD}-2) V to 2V	4-cell protection
VSS pin voltage level	3-cell protection
-0.3V or less	Prohibition of use

Cascade Connection by CTLC and CTLD Pins

When using cascade connection as shown in *the typical application circuit 2 of the APPLICATION INFORMATION chapter*, the R5651T can transfer each state of overcharge, overdischarge, and open-wire detections by connecting between the COUT and CTLC pins and between the DOUT and CTLD pins. When not using it, the CTLC and CTLD pins must be connected to VSS.

When the CTLC / CTLD pin voltage is higher than the value of High threshold voltage 1 (V_{CTLC1H} / V_{CTLD1H}), or when the CTLC / CTLD pin voltage is lower than the value of High threshold voltage 2 (V_{CTLC2H} / V_{CTLD2H}), the COUT / DOUT pin becomes High after normal operation.

When applying a voltage of between V_{CTLC1H} and V_{CTLC2H} to the CTLC pin, the COUT pin with an external pull-down resistor becomes Hi-Z forcedly, and when applying a voltage of between V_{CTLD1H} and V_{CTLD2H} to the CTLD pin, the DOUT pin with an external pull-down resistor becomes Low forcedly.

Don't make the CTLC and CTLD pins open. The following table indicates a relationship between the control pins (CTLC and CTLD) and the state of the external FETs for the COUT and DOUT pins.

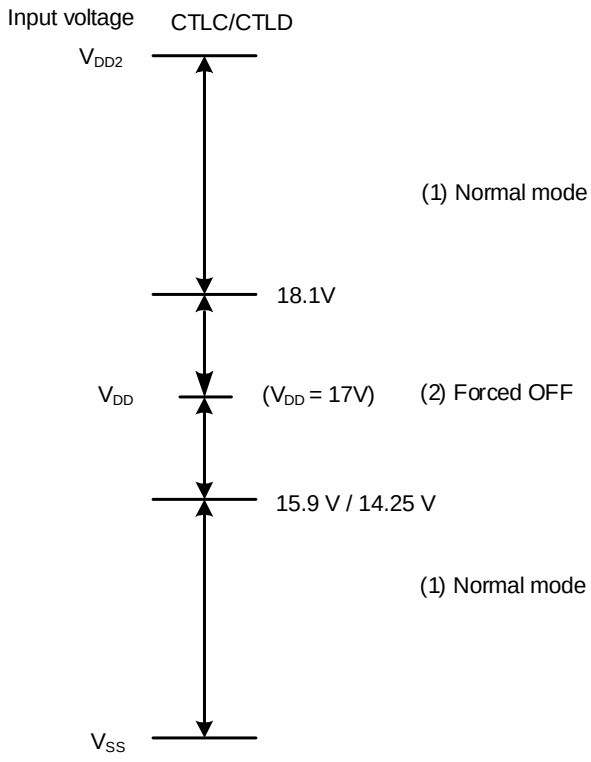
External FET's state by CTLx pins

CTLC / CTLD pins	External FET for COUT / DOUT pins
$2V_{DD}$ to V_{CTLC1H} / V_{CTLD1H}	ON (Normal operation)
V_{CTLC1H} / V_{CTLD1H} to V_{CTLC2H} / V_{CTLD2H}	Forced OFF
V_{SS} to V_{CTLC2H} / V_{CTLD2H}	ON (Normal operation)

When V_{DD} = 17 V (Refer to *"Electrical Characteristics"*),

V_{CTLC1H} / V_{CTLD1H}: Typ.18.1V

V_{CTLC2H} / V_{CTLD2H}: Typ.15.9 V / 14.25 V



Delay Time Setting by CT1 and CT2 pins

The CT1 and CT2 pins are used for setting each delay time of the overdischarge detection (t_{VDET2}), the discharge overcurrent detection 1 (t_{VDET31}) and the discharge overcurrent2 (t_{VDET32}) by connecting external capacitors C_{CTX}. Each of t_{VDET2}, t_{VDET31}, and t_{VDET32} be calculated by the equation of $CV = i\Delta t$.

	Min.	Typ.	Max.	Details
T_{VDET2} [µs]	2.52 × C_{CT1} [nF] When C_{CT1} = 33 nF, t_{VDET2} = 83 ms	3.6 × C_{CT1} [nF] When C_{CT1} = 33 nF, T_{VDET2} = 119 ms	4.68 × C_{CT1} [nF] When C_{CT1} = 33 nF, T_{VDET2} = 155 ms	Refer to the following a.
t_{VDET31} [ms]	2.1 × C_{CT2} [nF] When C_{CT2} = 3.3 nF, t_{VDET31} = 6.9 ms	3 × C_{CT2} [nF] When C_{CT2} = 3.3 nF, t_{VDET31} =9.9 ms	3.9 × C_{CT2} [nF] When C_{CT2} =3.3 nF, t_{VDET31} = 12.9 ms	Refer to the following b.
t_{VDET32} [ms]	0.21 × C_{CT2} [nF] When C_{CT2} =3.3nF, t_{VDET31} = 0.69 ms	0.3 × C_{CT2} [nF] When C_{CT2} = 3.3 nF, t_{VDET31} = 0.99 ms	0.39 × C_{CT2} [nF] When C_{CT2} = 3.3 nF, t_{VDET31} = 1.29 ms	Refer to the following c.

Details:

a: t_{VDET2} is given by the following expression, where are C_{CT1} = 33 nF, V_{DCT1} = 1.80 V, and I_{CT1} = 0.5 µA.

$T_{VDET2} = C_{CT1} \times V_{DCT1} / I_{CT1}$

T_{VDET2} = 119 ms

b: t_{VDET31} is given by the following expression, where are C_{CT2} = 3.3 nF, V_{DCT2} = 1.50 V, I_{CT2} = 500 nA.

$t_{VDET31} = C_{CT2} \times V_{DCT2} / I_{CT2}$

t_{VDET31} = 9.9 ms

c: t_{VDET32} is given by the following expression, where are C_{CT2} = 3.3 nF, V_{DCT2} = 1.50 V, I_{CT2} = 500 nA.

$t_{VDET32} = C_{CT2} \times V_{DCT2} / (I_{CT2} \times 10)$

t_{VDET32} = 0.99 ms

Temperature Protection by External NTC

The R5651T has three temperature detectors to protect the charge high temperature, the charge low temperature, and the discharge high temperature. The VR and the TEP pins are used to supervise the temperature. The VR pin supervises the temperature only for 10 ms in the 1 s period to reduce supply current between R_{TEP} and NTC.

In the discharged state, the discharge high temperature is detected when the supervised temperature exceeds T_{DDH}, and the DOUT pin becomes Low to stop the discharge current. After that, the discharge high temperature is released when the supervised temperature drops below T_{RDH}, and thereby the DOUT pin becomes High to permit discharging.

In the non-discharged state, the charge high temperature is detected when the supervised temperature exceeds T_{DCH}, and the COUT pin becomes Hi-Z to stop the charge current. After that, the charge high temperature is released when the supervised temperature drops below T_{RCH}, and thereby the COUT pin becomes High to permit charging. As with the high temperature, the charge low temperature is detected when the supervised temperature drops below T_{DCL}, and thereby the COUT pin becomes Hi-Z to stop the charge current. After that, the charge low temperature is released when the supervised temperature exceeds T_{RCL}, and thereby the COUT pin becomes High to permit charging.

The VMPD pin supervises the discharge current by its input voltage. After detecting the charge high / low temperature, these protected states are released immediately when the VMPD pin voltage (V_{VMPD}) exceeds V_{DSG}. Delay times for temperature protection are fixed internally. For the example of the discharge high temperature detection, the internal timer counts 64 ms until the discharge high temperature is detected. The detecting and releasing at other temperatures also are set at the same delay time.

In standby mode, the temperature protection does not work because the VRT pin is used to supply a voltage source for a voltage divider.

Reference resistance values for R_{TEP} and NTC [(1)]

- R_{TEP}: 33 kΩ ±1%
- NTC: 10 kΩ ±1% (Ta = 25°C, B-value($B_{25/85}$) = 3435K ±1%

COUT and DOUT pins setting for temperature protection

State	Pin	to 0°C (T_{DCL})	0°C (T_{DCL}) to 45°C (T_{DCH})	45°C (T_{DCH}) to 70°C (T_{DDH})	70°C (T_{DDH}) or more
Charge	COUT	Hi-Z	High	Hi-Z	Hi-Z
	DOUT	High	High	High	Low
Discharge	COUT	High			Hi-Z
	DOUT	High			Low

Open-wire Detection

Refer to *Typical Application Circuit 1 in Application Information* for details on the following descriptions.

(1) Refer to *Technical Notes on External Components* for recommended parts.

The R5651T for the three to five cells protection can detect open-wire at P1 to P7. When detecting an open-wire, the COUT and DOUT pins output Hi-Z and Low respectively.

The open-wire detection at P2 to P7 runs during approx.150ms in a cycle of t_{LT} (typ.4.00s). In the open-wire detection sequence for P2 to P5, the EVEN_SW and ODD_SW signals turn on the switch between VC1 and VC2, VC3 and VC4, or VC5 and VSS and the switch between VC2 and VC3 or VC4 and VC5 alternately to detect the open-wire. The IC's internal impedance in between pins that the switch is on drops for approx.64ms. When the open-wire occurs, the VCx pin voltage varies due to a difference between the internal impedances. The IC detects the variations in voltages and enters the open-wire detecting state. When the voltage of [VCn－VCn+1 (n = 1,2,3,4)] or [VC5－VSS] is the open-wire disable threshold (V_{DIn}) or less during the open-wire detection, the IC does not judge detection / release to the open-wire.

The open-wire at P6 is detected when V_{SS} exceeds V_{SENSE} and the VSS open-wire detection disable threshold (V_{DSL}), and the open-wire at P7 is detected when V_{SENSE} drops below V_{SS} and V_{DSL}. The open-wire detecting state is released by a shift to the standby state.

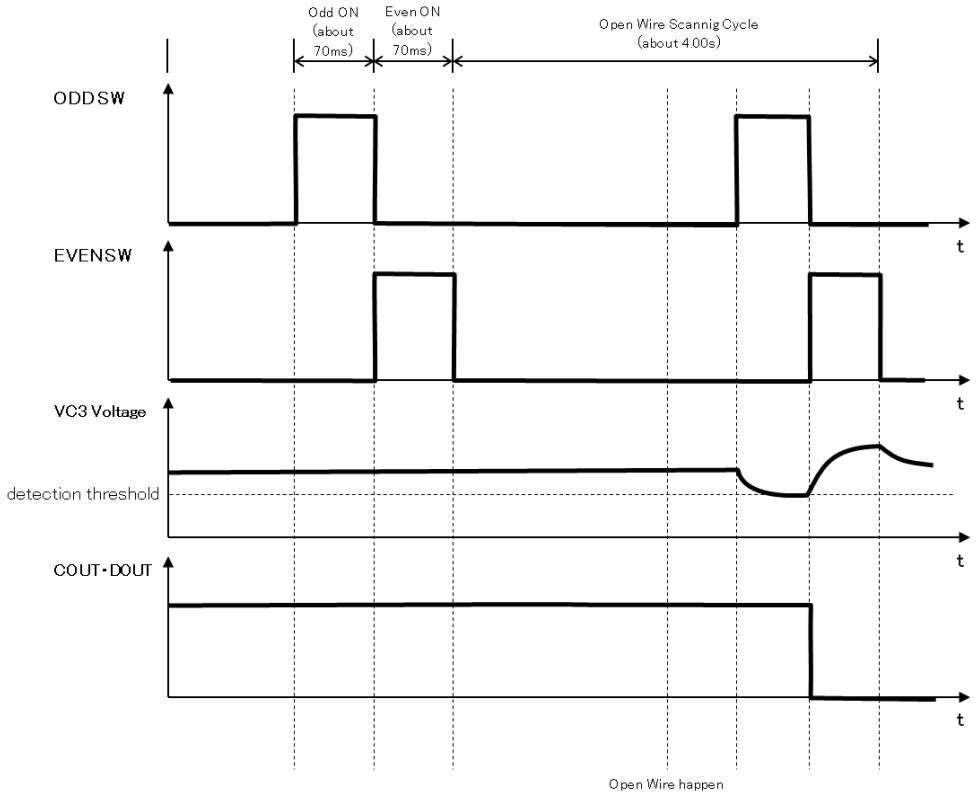
Even if the battery voltage is higher than V_{DIn}, the open-wire detection might not occur when the voltage of [VCn－VCn+1 (n = 1,2,3,4)] or [VC5－VSS] drops below V_{DIn} at the open-wire. When the battery voltage drops below the 0 V battery charging inhibition voltage (V_{NOCHG}) by a drop of the battery voltage, the COUT pin might become Low by detecting the 0V battery charging inhibition.

【limitations】

The following limitations are required for the open-wire detection at P2 to P7.

- In the case that the open-wire detection period occurs in the overcharge / overdischarge detection delay time counting states, the open-wire detection does not run, the overcharge / overdischarge detection with the higher priority is handled first, and the open-wire detection runs during the next period. Thereby, a delay time for the overcharge / overdischarge detections might become longer.
- In the case that the voltage of [VCn－VCn+1 (n = 1,2,3,4)] or [VC5－V_{SS}] is nearby the open-wire disable threshold (V_{DIn}), it is impossible to detect an open-wire due to the individual difference of a IC, a battery voltage balance, operating conditions, and external components.
- The open-wire at P7 is not detected when connected a load between Pack+ and Pack-. In the recommended circuit, a discharge via the load between Pack+ and Pack- does not occur because of no discharge path at P7. Even the space between them is open, the open-wire is not detected.
- The open-wire at P7 is not detected when the COUT pin is Hi-Z, even a charger is connected between Pack+ and Pack-.
- Regarding the open-wire at P7, the discharge / charge overcurrent might be detected by a pulled-up of the SENSN pin with an internal circuit in the R5651T.
- The release from the open-wire detection at P6 and P7 might not occur unless the charger is removed and the VMPC pin voltage (V_{VMPC}) exceeds the power on voltage at standby mode (V_{STB}).

Timing Charts

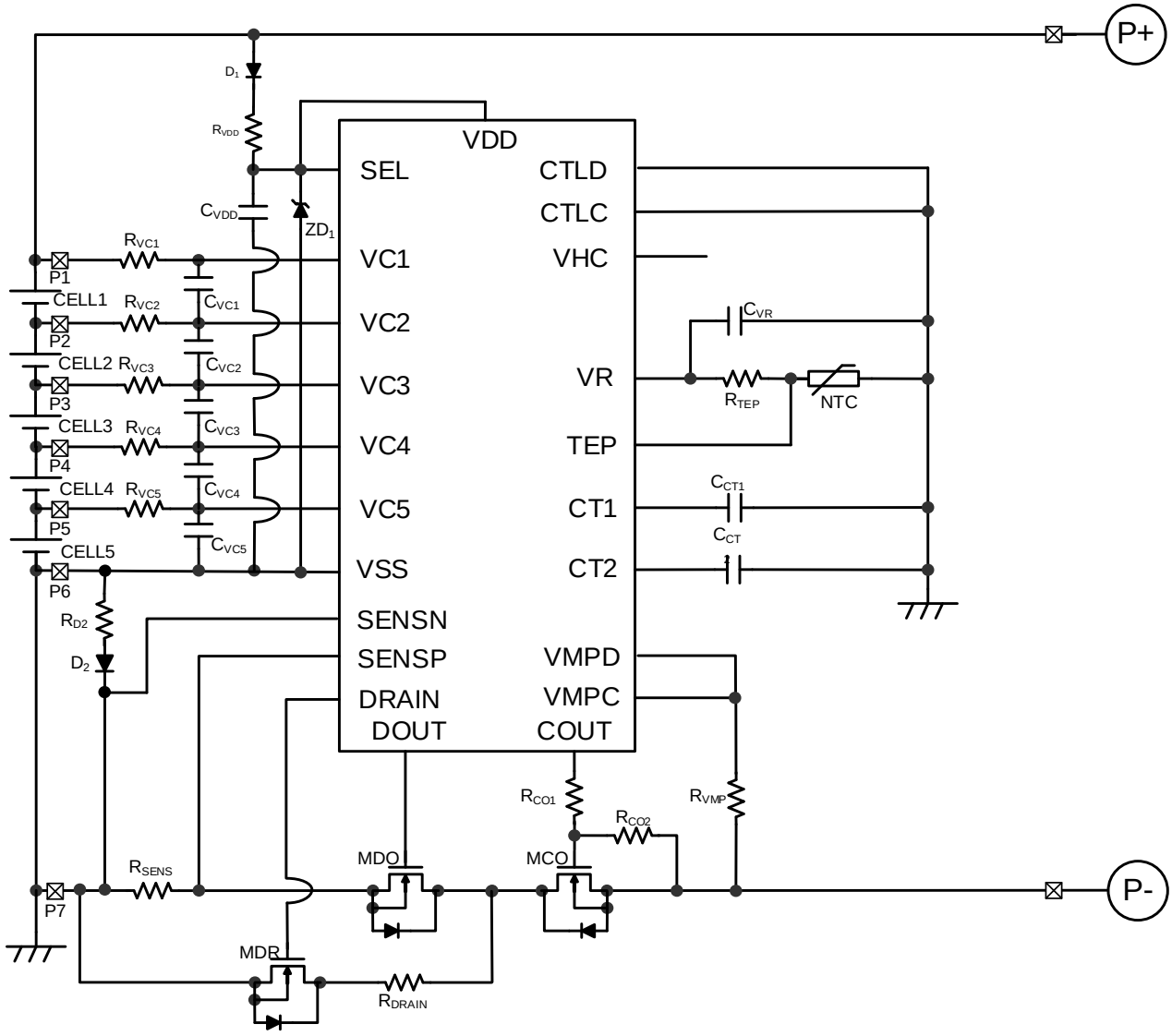


Open-wire Detection Timing Diagram (High output type at detection)

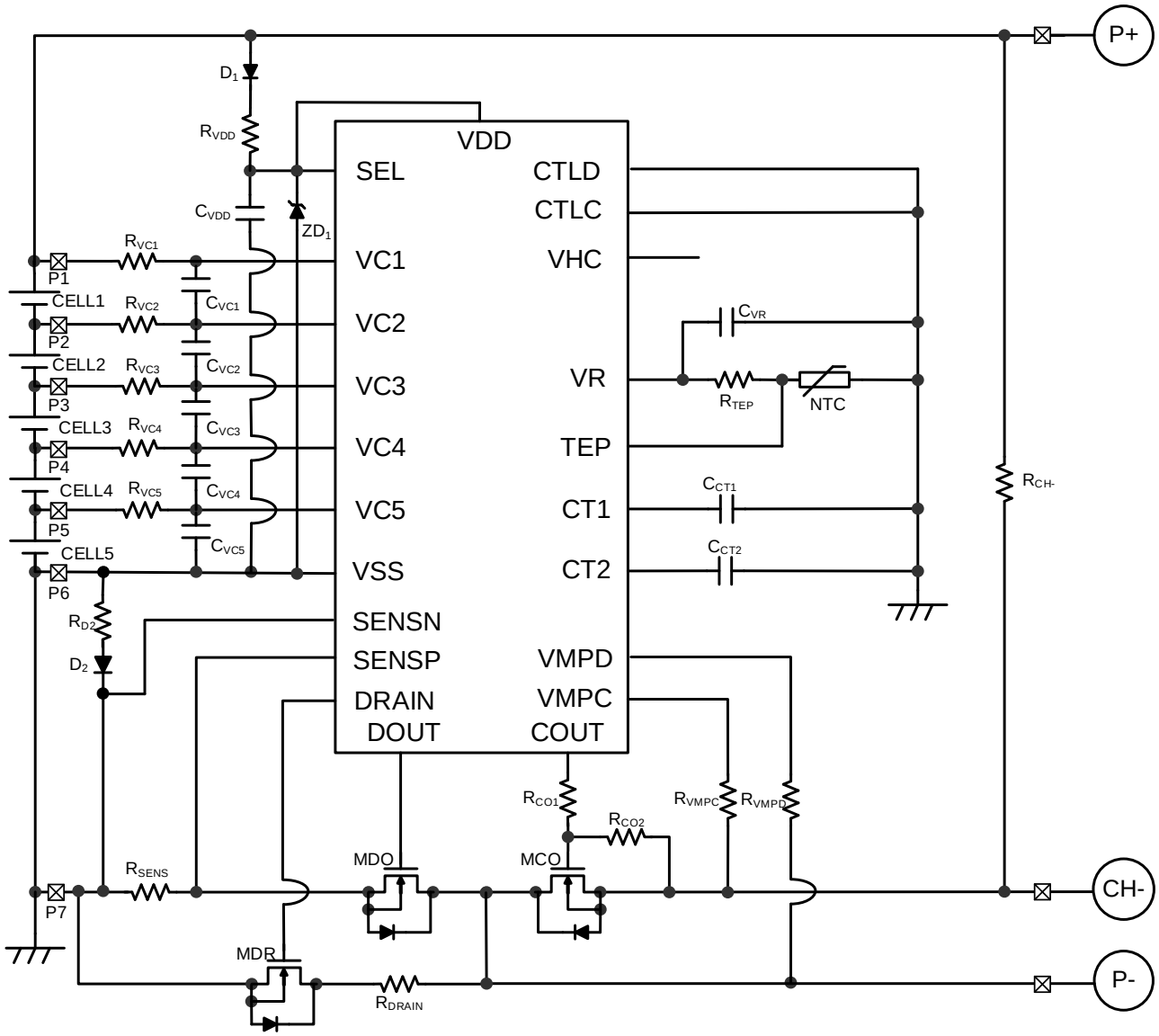
APPLICATION INFORMATION

Typical Application Circuits

When the FET connected to the COUT pin is turned off and a load is connected between Pack+ and Pack-, the discharge current is applied via the parasitic diode of its FET. When the FET connected to the DOUT pin is turned off and a charger is connected between Pack+ and Pack-, the charge current is applied via the parasitic diode of its FET. Thus, the FETs must be enough to flow the current.

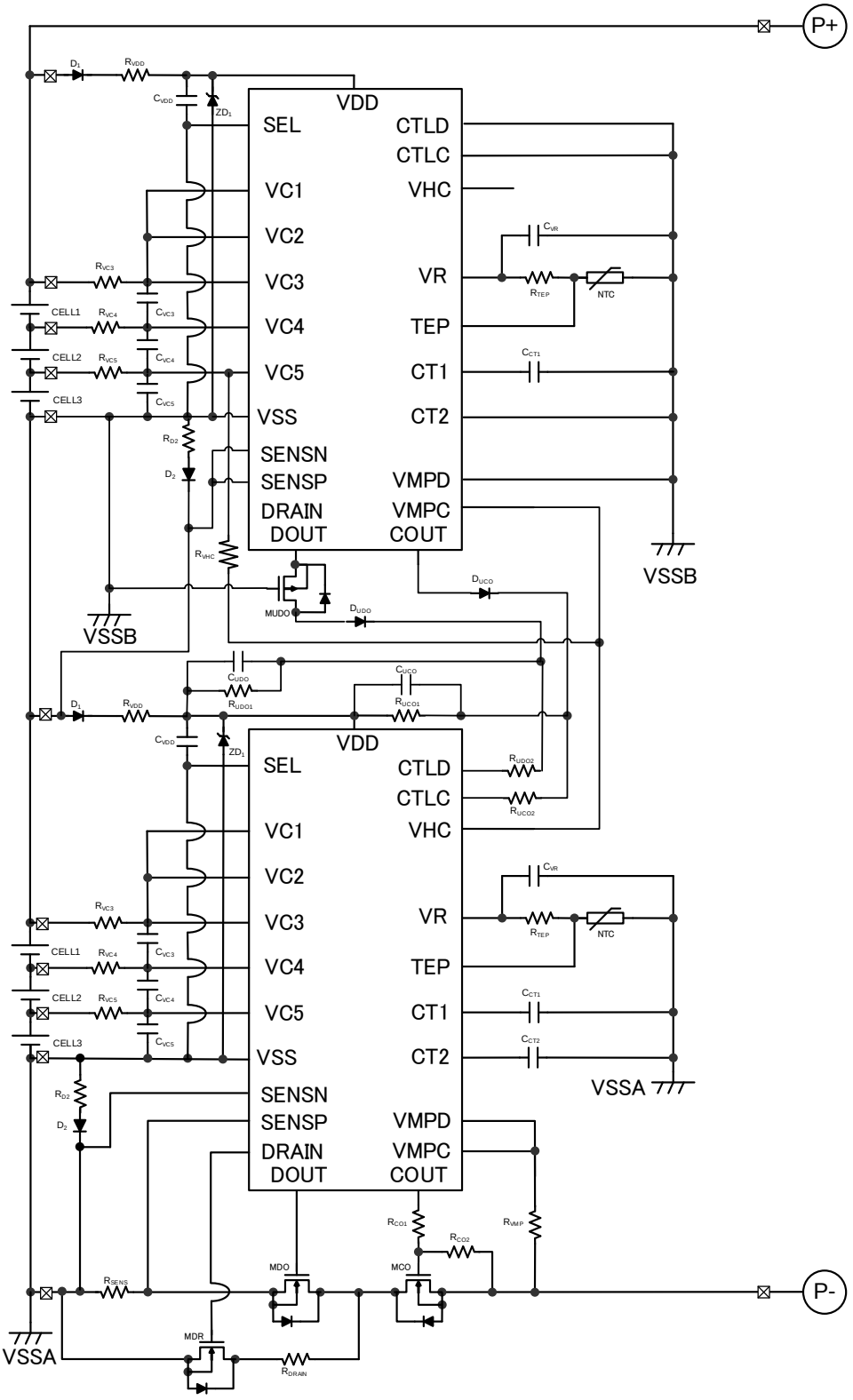


Typical Application Circuit for 5-cell Protection Battery Charger

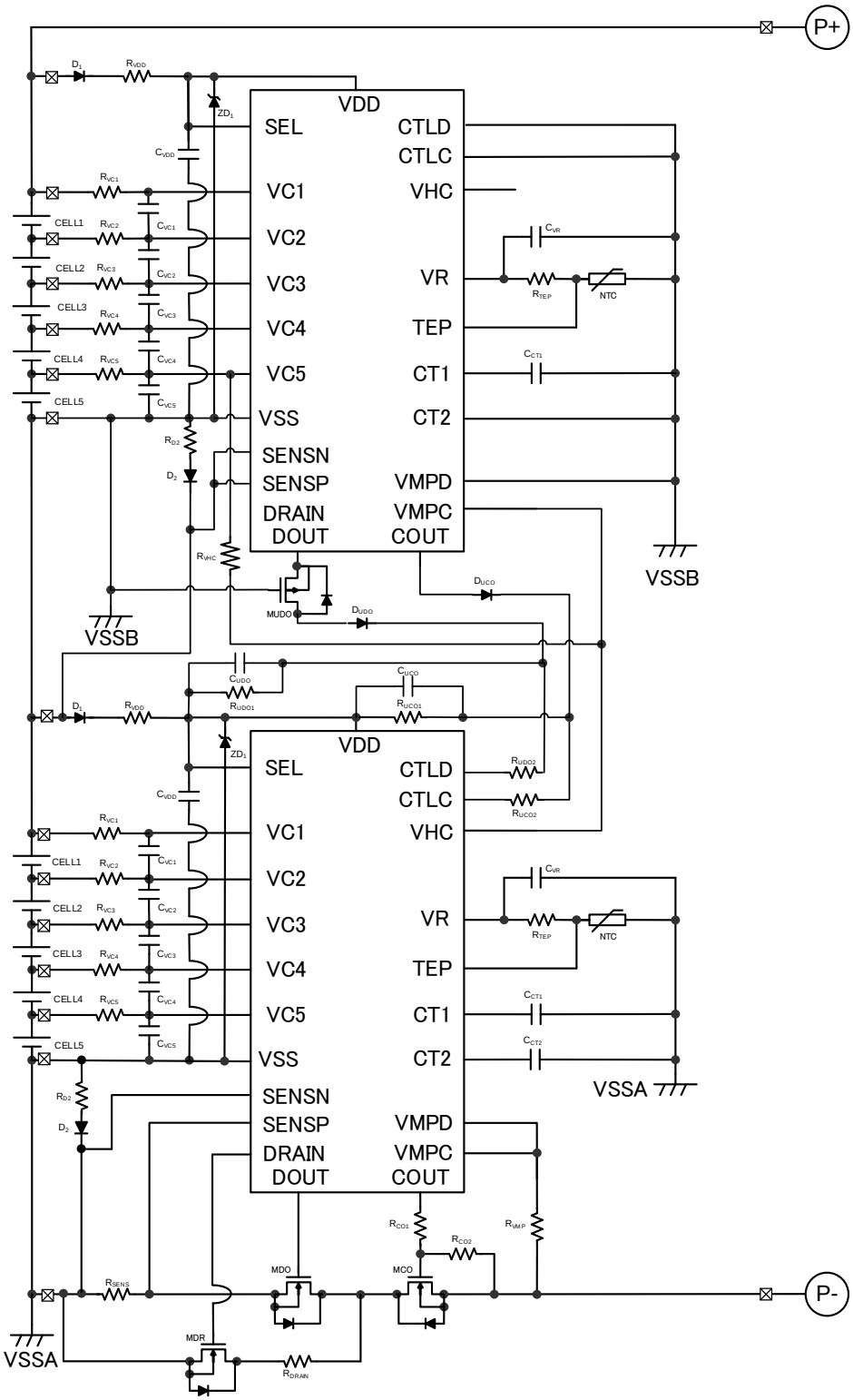


Typical Application Circuit for 5-cell Protection Battery Charger

(When separated between charging and discharging paths)



Typical Application Circuit for 6-cell Protection Battery Charger



Typical Application Circuit for 10-cell Protection

External Components Selection Guide

Symbol	Value (Typ.)	Range	Unit	Remarks [1]
R_{VDD}	1	1	kΩ	Refer to *Technical Note [1]*.
R_{VC1} / R_{VC2} / R_{VC3} / R_{VC4} / R_{VC5}	1	1	kΩ	Refer to *Technical Note [2]*.
R_{SENS}	10	1 or more	mΩ	Depending on set value for overcurrent.
R_{DRAIN}	75	*Note [3]*	kΩ	Refer to *Technical Note [3]*.
R_{CO1}	1	*Note [3]*	MΩ	
R_{CO2}	2.2	*Note [3]*	MΩ	
R_{UCO1}	6	2 to 8	MΩ	Recommended for the accuracy of 1%. Refer to *Technical Note [6] and [14]*.
R_{UCO2}	10	10	kΩ	Refer to *Technical Note [13]*.
R_{UDO1}	6	2 to 8	MΩ	Recommended for the accuracy of 1%. Refer to *Technical Note [14]*.
R_{UDO2}	10	10	kΩ	Refer to *Technical Note [13]*.
R_{VHC}	4.7	4 to 6	MΩ	Refer to *Technical Note [5]*.
R_{VMP}	10	0.01 to 10	MΩ	Refer to *Technical Note [7]*.
R_{D2}	-	-	Ω	Refer to *Technical Note [12]*.
C_{VDD}	1	0.1 to 1.0	µF	Refer to *Technical Note [1] and [14]*.
C_{VC1} / C_{VC2} / C_{VC3} / C_{VC4} / C_{VC5}	0.1	0.1	µF	Refer to *Technical Note [2]*.
C_{CT1}	2.2	1 or more	nF	-
C_{CT2}	3.3	1 or more	nF	Refer to *Technical Note [4]*.
C_{VR}	0.1	0.1	µF	-
C_{UCO}	22	22	nF	Refer to *Technical Note [14]*.
C_{UDO}	22	22	nF	Refer to *Technical Note [14]*.
ZD_1	30	Up to 30	V	Refer to *Technical Note [8]*. Recommended Component Number: MM1Z30 0.5W 30V J SOD-123 EIC
R_{TEP}	33	33	kΩ	-
R_{CH-}	22	22 or more	MΩ	-
NTC	10	10	kΩ	Recommended Component Number:103AT-4-040 (SEMITEC) NTCG103JF103F / NTCG163JF103F(TDK)
D_1	−	−	−	Refer to *Technical Note [11]*.
D_2	−	−	−	Refer to *Technical Note [12]*.
D_{UCO}	−	−	−	Refer to *Technical Note [14]*.
D_{UDO}	−	−	−	Refer to *Technical Note [14]*.
MCO	−	−	−	Refer to *Technical Note [9]*.
MDO	−	−	−	
MDR	−	−	−	Refer to *Technical Note [10]*.
MUDO	−	−	−	Refer to *Technical Note [14]*.

[1] Refer to "*Technical Notes for External Components*" for details.

Technical Notes on the Selection Components

【1】R_{VDD} stabilizes voltage fluctuations of the IC in conjunction with C_{VDD}.

【2】In the case that a large R_{VCx} is set to stabilize the voltage fluctuations with conjunction with C_{VCx}, the detection voltage becomes High because of the internal conduction current of the IC.

【3】Each resistor of R_{DRAIN}, R_{CO1} and R_{CO2} requires an appropriate value as to satisfy the next equation. Otherwise, it might be impossible to release from the discharge overcurrent and the short-circuit.

$$R_{DRAIN} < V_{REL3} \times (R_{CO1} + R_{CO2})/(V_{DD} - V_{REL3})$$

In the case that a small R_{CO1} / R_{CO2} is set, the supply current of protection circuit board increases when the output of COUT is High. In the case that a large R_{CO1} / R_{CO2} is set, the speed pulled-down of the FET gate for charge becomes slow when the COUT pin is Hi-Z, thereby it takes much time to turn the FET off.

【4】When a too small C_{CT2} is set, the discharge overcurrent detection delay time 1 / 2 (t_{VDET31} / t_{VDET32}) becomes shorter than the short-circuit delay time (t_{SHORT}).

【5】In the case of the cascade connection, the VHC pin on a lower voltage IC transmits a presence / absence of load connection and charger connections to a higher voltage IC.

【6】R_{UCO1} must be set to satisfy R_{UCO} = R_{CO1}+R_{CO2}. In the case that an extremely large resistor is set, the CTLC pin might not be pulled down by the dividing resistance at the COUT pin of Hi-Z. In the case that a small resistor is set, the consumption current via R_{UCO} increases when the COUT pin is High.

【7】When a large resistor for R_{VMP} is set, a sufficient consideration must be given to noise to a wire between the resistor and the IC. The resistor of R_{VMP} should be placed as close as possible to the VMPC pin to reduce noise.
In the case of the cascade connection, the VMPC and VMPD pins are pulled up via R_{VMP} to the top cell when the DOUT pin is turned off, thereby the current flows via R_{VMP} and the internal diode. For this reason, appropriate value for R_{VMP} must be set.

【8】It is recommended to connect a Zener diode in order to prevent a high voltage to the IC. The Zener diode must be directly connected between the VDD and VSS pins.

【9】The charge control FET (MCO) and the discharge control FET (MDO must make a sufficient consideration to their maximum voltage tolerance, current rating, maximum power consumption and peak consumption when short-circuit.

【10】The pull-down FET (MDR) must make a sufficient consideration to its maximum voltage tolerance.

【11】The diode of D_1 prevents a drop in the VDD pin voltage (V_{DD}) along with a steep drop of the battery voltage during the short-circuit.

【12】The diode of D_2 prevents a boost of the VSS when an open-wire between the minus side of the CELL3 and the VSS pin. Thereby it is possible to turn on / off the MDO being a FET for the DOUT pin even when the open-wire. When the open-wire between the minus side of the CELL3 and VSSA is detected, RD2 limits the current applied to D_2. D_2 and R_{D2} must design so that a forward voltage to diode is 0.4V or more and the MDO gate threshold voltage or less, at 25°C and 85°C. When connecting two diodes for D_2 in serial, it might meet the above conditions at low cost in some instances.

【13】If the maximum input voltage exceeds 30V, a resistor must be inserted to prevent permanent damage to the IC. It is recommended to place the resistor nearby the CTLC / CTLD pin to reduce the influence as possible.

【14】In the case of a battery with a high impedance, the battery might cause a steep change in voltage when connected with loads. External components of R_{UDO1}, R_{UCO1}, C_{UDO}, C_{UCO}, DUDO, DUCO, and MUDO for the cascade connection have effect to prevent misdetection when a high output voltage of the COUT / DOUT pin on the higher voltage IC drops below the CTLC / CTLD threshold voltage 1 (V_{CTLC1H} / V_{CTLD1H}) on the lower voltage IC.

Refer to the following table for external component values and examples of a transmission delay time at the cascade signal of Low according to their components.

Cells Count	C_{UDO},C_{UCO} [nF]	R_{UDO1},R_{UCO1} [MΩ]	CTLD pin input delay time (t_{CTLD}) [s]	CTLC pin input delay time (t_{CTLC}) [s]
6	22	6	0.17 to 0.49	0.17 to 0.50
10	22	6	0.23 to 0.49	0.23 to 0.57

The conditions calculated above values are as follows:

V_{DET1} = 4.22 V, V_{DET2} = 2.6 V, C_{VDD} on the lower voltage IC = 0.1 µF, and the battery voltage of 1.3 V or more at load connection

TECHNICAL NOTES

A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Please evaluate the product at the PCB level before use, as some symptoms may remain that cannot be confirmed by the evaluation at the IC level.
- When using any coating or underfill to improve moisture resistance or joining strength, evaluate them adequately before using. In certain materials or coating conditions, corrosion by contained constituents, current leakage by moisture absorption, crack and delamination by physical stress can happen. If the curing temperature of the coating material or underfill material exceeds the absolute maximum rating, the electrical characteristics of this product may change.
- When performing X-ray inspection in mass production process and evaluation build stage such as the product functions and characteristics confirmation, please confirm X-ray irradiation does not exceed 1.5Gy (absorbed dose for air).

PD-TSSOP-24-(85125)-JE- A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51.

Measurement Conditions

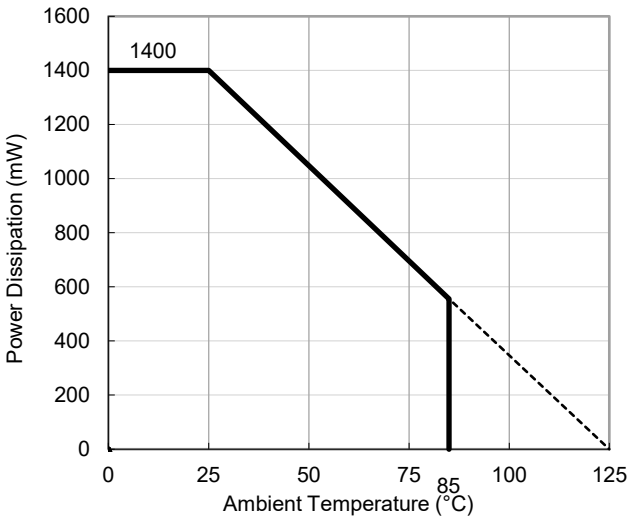
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layer (First Layer): Less than 10% of 62 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 74.2 mm Square Outer Layer (Fourth Layer): Less than 10% of 62 mm Square
Through-holes	None

Measurement Result (Ta = 25°C, Tjmax = 125°C)

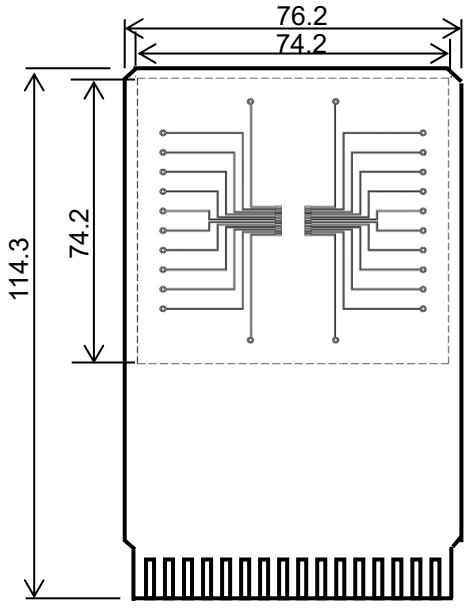
Item	Measurement Result
Power Dissipation	1400 mW
Thermal Resistance (θja)	θja = 71°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 20°C/W

θja: Junction-to-Ambient Thermal Resistance

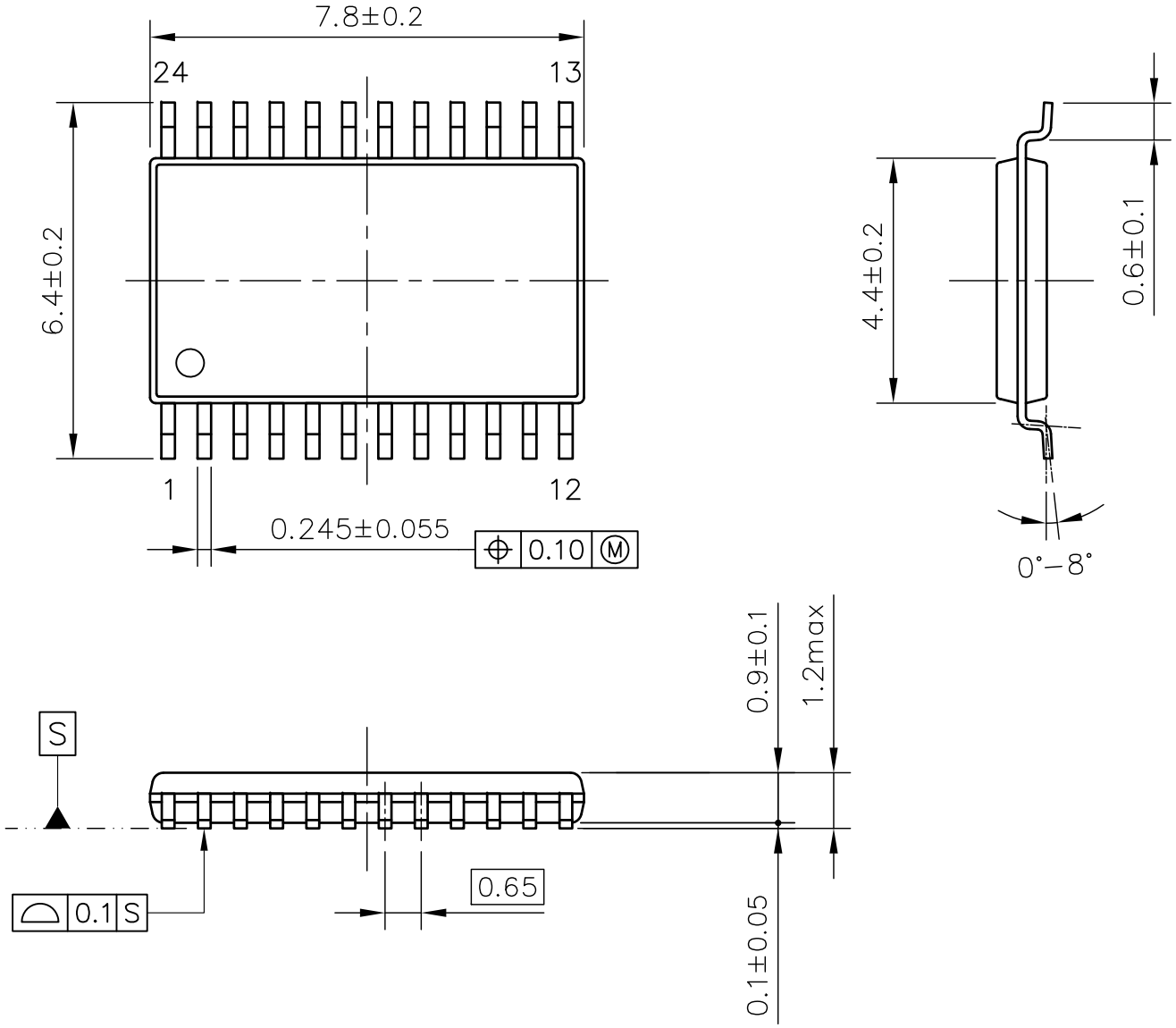
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



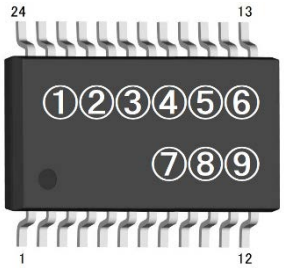
Measurement Board Pattern



TSSOP-24 Package Dimensions (Unit: mm)

①②③④⑤⑥: Product Code ⋯ Refer to Part Marking List

⑦⑧⑨: Lot Number ⋯ Alphanumeric Serial Number



R5651T (TSSOP-24) Part Markings

R5651T Part Marking List

Product Name	① ② ③ ④ ⑤ ⑥
R5651T103CA	H 1 0 3 C A
R5651T104CA	H 1 0 4 C A

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
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4. The technical information described in this document shows typical characteristics of and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under our company's or any third party's intellectual property rights or any other rights.
5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, telecommunication equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death (aircraft, spacevehicle, nuclear reactor control system, traffic control system, automotive and transportation equipment, combustion equipment, safety devices, life support system etc.) should first contact us.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. Anti-radiation design is not implemented in the products described in this document.
8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.
11. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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